





### **Cramming the H into HBM**

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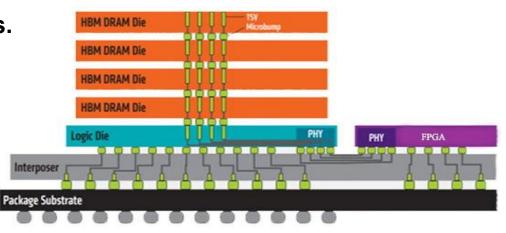
SKA Low Correlator & Beamformer

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## **High Bandwidth Memory (HBM)**



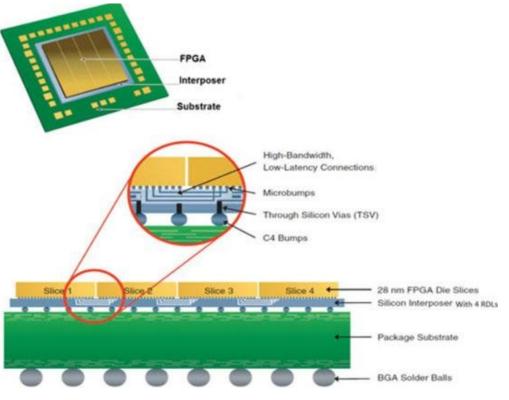
- HBM is a new type of memory chip.
- Vertically stacked memory chips interconnected by Through Silicon Vias (TSV).
- Low power consumption.
- Ultra wide communication lanes.
- Faster speed.
- Less Area.



# Stacked Silicon Interconnect (SSI)

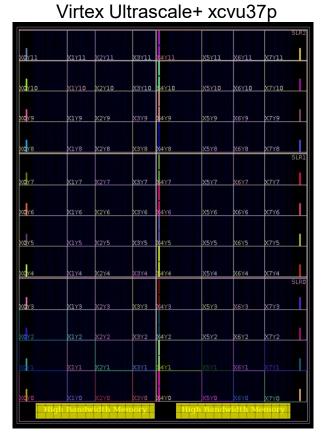


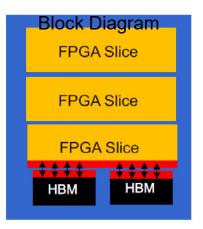
- 3-D Packaging approach
- Combines multiple Super Logic Region (SLR) components mounted on a passive Silicon Interposer.
- SLR contains
  - Input LUTs, Registers, I/O components, Block Memory, DSP blocks, etc...
- Multiple SLR components are stacked next to each other to create the SSI device.



### **FPGA** with **HBM**





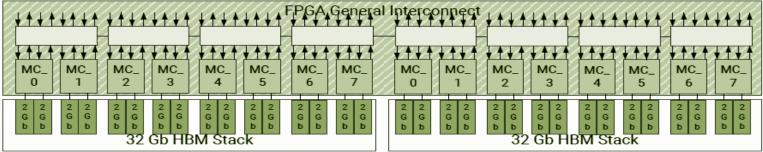




- HBM is added as a slice.
- SLR0 serves as a master.
- HBM comes with DA ports which have to be routed to BGA balls.

# HBM in virtex ultrascale + devices



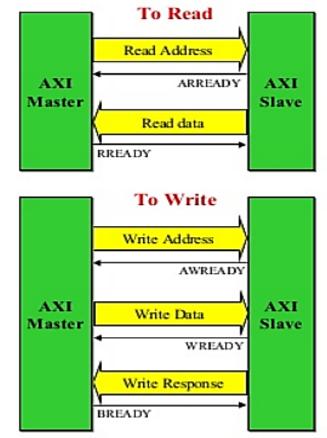


- Divided into two 1024-bit wide HBM stacks.
- Each stack is split into eight independent memory channels.
- Each Memory channels has two 64-bit pseudo channels.
- Each memory channel can be operate at an independent clock rate.
- AXI3 Protocol is used.
- It has a 16 × 16 AXI crossbar switch.

### **Basic AXI transactiton**

- The AXI (Advanced eXtensible Interface) is a point to point interconnect that designed for high performance, high speed microcontroller systems.
- It avoids bus sharing and therefore allow higher bandwidth and lower latency.
- The procedure for the AXI protocol is as follows:
  - Master & slave must "handshake" to confirm valid signals
  - Transmission of control signal must be in separate phases
  - Separate channels for transmission of signals
  - Continuous transfer may be accomplished through burst-type communication







IBM Configuration Selection Example	nple Design Options Address Map Options Reorder,Refresh and Power Sav	rings O 4 1
Component Name	hbm_0	
HBM Density 4GB 🗸 Select Sta	ack LEFT v	
otal Available Memory(MB)	4096	
Enable Switch 0/Global Addressing	Stack 0	
nable & Configure all MCs to Same Va	ue? yes 🗸	
Memory Clocking		
HBM Memory Frequency for Stack0 (M	Hz) 900 🐵 [225 - 900]	
PLL Reference Input Clock 0 (MHz)	100 ~	
APB Clocking		
APB Interface 0 Clock (MHz)	100 🐵 [50 - 100]	
Temperature Polling Interval on APB-0	(ms) 1.0 (b) [1.0 - 1000.0]	
Select MC's to Enable for Stack0		
✓ MC 0 ✓ MC 1 ✓ MC 2 ✓ MC	3 @ MC 4 @ MC 5 @ MC 6 @ MC 7	
Select AXI Slaves to Enable for Sta	ck 0	
✓ SAXI_00 ✓ SAXI_01 ✓ SAXI_02	♥ SAXI_03 ♥ SAXI_04 ♥ SAXI_05 ♥ SAXI_06 ♥ SAXI_07	
SAXI_08 SAXI_09 SAXI_10	SAXI_11 SAXI_12 SAXI_13 SAXI_14 SAXI_15	
Switch Clock Select 0		
Clock Select 0 AXI 07 ACLK 🗸		
Select Line Rate for each MC of St	ack 0	(
MC0 div4 ~		



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FPGA General Interconnect

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Enable & Configure all MCs to Same Value?		yes	~		MC_ M( 0 1	2 3 4
Memory Clocking					2 2 2 G G G b b b	2 2 2 2 2 2 2 2 2 G G G G G G G G G G G
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APB Clocking						
APB Interface 0 Clock (MHz)	100	D	@ [50 -	100]		
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Select MC's to Enable for Stack0						
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Select AXI Slaves to Enable for Stack	0				SAVI 06	SAXI_07
Select AXI Slaves to Enable for Stack		_03 SAXI_04	SA)	₫_05 🕑	3403_00	1000





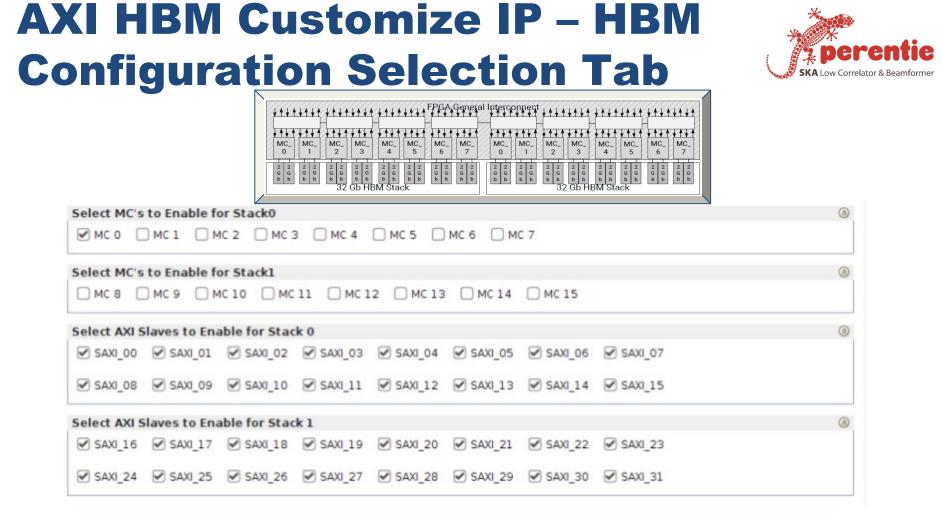
Enable & Configure all MCs to Same Value?	yes	~	
Memory Clocking			6
HBM Memory Frequency for Stack0 (MHz)	900 ©	[225 - 900]	
PLL Reference Input Clock 0 (MHz)	100 ~		
APB Clocking			6
APB Interface 0 Clock (MHz)	100	© [50 - 100]	
Temperature Polling Interval on APB-0 (m	s) 1.0	☺ [1.0 - 1000.0]	
Select MC's to Enable for Stack0			6
✓ MC 0 □ MC 1 □ MC 2 □ MC 3	□ MC 4 □ MC 5	□ MC 6 □ MC 7	
Select AXI Slaves to Enable for Stack	0		6
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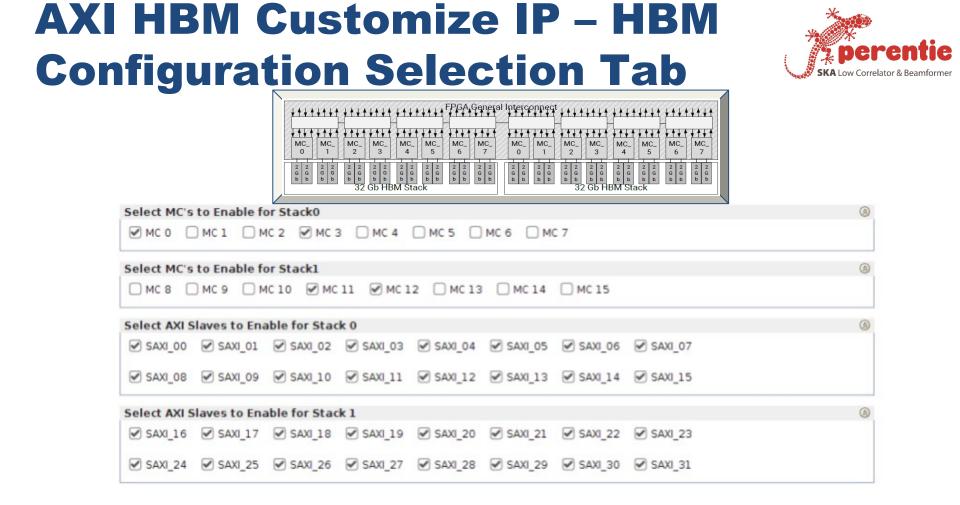


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Enable & Configure all MCs to Same Value	yes 🗸	
Memory Clocking		8
HBM Memory Frequency for Stack0 (MHz)	900 🐵 [225 - 900]	
PLL Reference Input Clock 0 (MHz)	100 ~	
APB Clocking		8
APB Interface 0 Clock (MHz)	100 (50 - 100)	
Temperature Polling Interval on APB-0 (m	) 1.0 (1.0 - 1000.0)	
Select MC's to Enable for Stack0		۲
✓ MC 0	□ MC 4 □ MC 5 □ MC 6 □ MC 7	
Select AXI Slaves to Enable for Stack	0	8
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SAXI_08 SAXI_09 SAXI_10 (	SAXI_11 SAXI_12 SAXI_13 SAXI_14 SAXI_15	



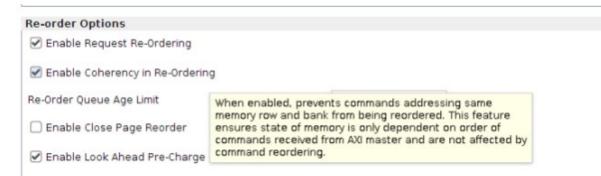
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HBM Den	sity 8GB	~						
Total Ava	ilable Memory	(MB)	8	92				
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Enabl	e Switch 1/Glo	bal Addressin	g Stack 1					
Enable &	Configure all	MCs to Same '	Value? v	es	~			
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elect MC's	to Enable f	or Stack1						(8
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elect AXI S	laves to En	able for Stat	:k 0					(8
SAXI_00	SAXI_01	SAXI_02	SAXI_03	SAXI_04	SAXI_05	SAXI_06	SAXI_07	
SAXI_08	SAXI_09	SAXI_10	SAXI_11	SAXI_12	SAXI_13	SAXI_14	SAXI_15	
elect AXI S	laves to En	able for Sta	:k 1					(8
SAXI_16	SAXI_17	SAXI_18	SAXI_19	SAXI_20	SAXI_21	SAXI_22	SAXI_23	
SAXI 24	SAXI 25	SAXI 26	SAXI 27	SAXI 28	SAXI 29	SAXI 30	SAXI 31	







nfiguration Selection Exa	mple Design Options	Address Map Options	Reorder, Refresh and Power Savings Options	4 Þ
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Select Traffic Pattern Use	er Defined 🗸 🗸			
Re-order Options				8
Enable Request Re-Ord	ering			
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# Basic settings required to run the simulation

2-	Simulation										
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> Window Behavior											
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- Supported simulators: Modelsim, QuestaSim, IES and Verilog Compiler.
- Change the Compiled library location to the location of the compiled library in the installation area.
- In the Simulation tab, in the modelsim.simulate.vsim.more\_options enter +notimingcheck.
  - For <u>Questa simulator</u>, add +notimingchecks in Compilation tab questa.compile.vlog.more\_options and in the Simulation tab questa.simulate.vsim.more\_options.
  - For <u>IES simulator</u>, add -notimingchecks in the Elaboration tab ies.elaboration.ncelab.more\_options.

# Basic settings required to run the simulation

Simulation Specify various	settings assoc	iated to Simula	tion			2				
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	oge.									
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modelsim.s	imulate.custo	m_wave								
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### **Performance Measured**

#### (Mco, saxi\_00, clk - 450 Mhz)



Burst Len	Sequen	tial access pattern (rea	d and write)	Sequential write and Random read access pattern
Durst Len	Throughput (Gbps)	write only Throughput (Gbps)	read only Throughput (Gbps)	Throughput (Gbps)
1	24 (20%) (12Rd + 12Wr)	54 (47%)	54 (47%)	18 (15%) (9Rd + 9Wr)
2	42 (37%) (21 Rd + 21 Wr)	106 (92%)	105 (91%)	24 (20%) (12Rd + 12Wr)
4	50 (43%) (25 Rd + 25 Wr)	107 (93%)	105 (91%)	46 (40%) (23Rd + 23Wr)
8	84 (73%) (42 Rd + 42 Wr)	107.2 (93%)	105 (91%)	80 (69%) (40Rd + 40Wr)
16	106 (92%) (53 Rd + 53 Wr)	107.2 (93%)	105 (91%)	104 (90%) (52Rd + 52Wr)

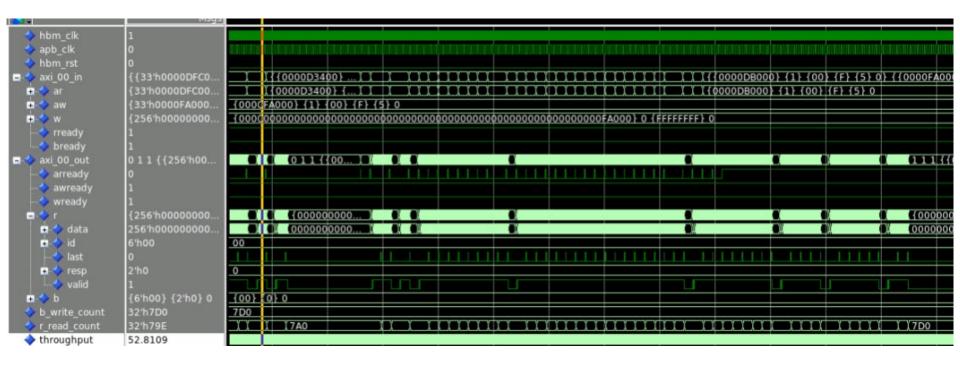
### Simulation result for Sequential access pattern(1MB of data, Burst length = 16)



												_						
🔷 hbm_clk	1																	
🔷 apb_clk	1	www	www	huun	JUUU	mm	mm	MM	mm	JUUU		mm	MM		mm		mm	MMM.
hbm_rst	0																	
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r_read_count	32'h793	<u>(788 78</u>	9 (7 <b>BA</b> (7B	3 (7BC )	BD 7B	E (7BF (	7C0 70	1 7C2	<u>7C3 (</u> 7	C4 (7C5	(7C6)	7C7 7C7	8 7 7 8	(7CA)(7	CB 7CC	(7CD)	7CE (7C	F (7D0
🔷 throughput	54.8519																	

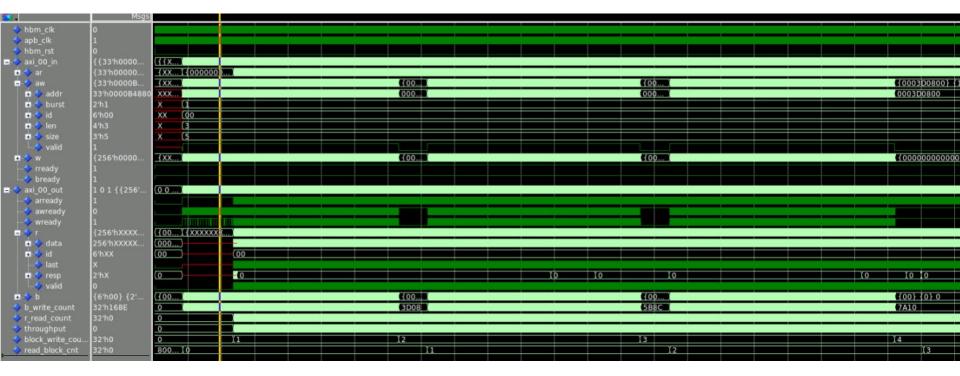
## Simulation result for Random read perentie and Sequential write pattern

(1MB of data, Burst length = 16)



## Simulation result for Random read perentie and Sequential write pattern

(Block size = 1MB, Burst length = 4)



## Simulation result for Random read and Sequential write pattern

(Block size = 1MB, Burst length = 16)

<u>.</u> .	Msgs																						
hbm_clk	1																_						
apb_clk	1																						
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# **Questions / Discussion?** Thank-you!