Why Model?

The rationale behind a systematic approach for modelling the Central Signal Processor

David Wilson Dept of Engineering, Computing & Mathematical Sciences AUT University



Why we need a model

To show the algorithm works To justify that the simplifications are reasonable Assist the low-level hardware designers Assist in debugging

Check cooling & thermal stresses





Key considerations

- Models at a suitably high-level abstraction
- Models are parameterised
 - Easy to adjust as req'mts change
 - Proof of concept
- Using Simulink/Matlab
- Built from components
 - Allow "plug & play"
 - "Model variants" in Simulink & projects



Basic block diagram of the Central Signal Processor



by a brownish arrow







Note: There are three second stage fine filterbanks (Cor/PSS/PST), each with a different frequency resolution; Fc, Fs, Ft - channels. Each Cor/BF engine operates on a different fine frequency slice. Repeat Correlator Fc-channels. Repeat Search BF Fs-channels, Repeat Timing BF Ft-channels.









Signal flow model

- Constructed in Simulink & Matlab
- Well suited to a block diagram approach
- Simulink well suited for operating in "frames"
- Possible to setup for group working (version & control)
- Expensive
- Awkward with multiple software versions





CSP Signal flow model





8

CSP Signal processing model





Computing for SKA 11-12th Feb 2016

Components



Computing for SKA 11-12th Feb 2016





Prototyping: From sketch to block diagrams



11







Frame-based processing







Oversampling

Oversampling is a key concept in the CSP. Necessary to obtain the required freq. response. We oversample at 27/32

Elegant & "mistake-free" using frames in Simulink





Figure 11: Oversampling at 27/32



¶

F-part with "pure" FFT

*	CSP_dataflow/F part * - Simulink
File Edit View Display Diagram Simulation	Analysis Code Tools Help
🖎 • 📄 💠 🔶 🔛 🏟 • 🚍 • 剩 🍕	▶ ■ ✓ 100 Normal ✓ ✓ … ▼
Model Browser [★] [■] Telescopes × F part	×
▲ CSP_dataflow ● Hide/Show Explorer Bar	CSP_dataflow ▶ 🖻 F part
Pa F part Pa Telescopes Pa X mu ⁺⁺ →	
▶a sum	
double [4096x1]	bwin double [4096x1] FFT double (c) [4096x 4 double (c) [1024x1]
le [4096x1]	[4096x1] [4096x1] V [1024x1]
	/indow FFT Downsample N
F	Take 1:4:end
	Doesr



15

X-part (embedded Matlab code)



Command Window

Computing for SKA 11-12th Feb 2016



Incoming signal generators

Uncorrelated Gaussian random noise (sampled)

Various pure tones (summed)





Computing for SKA 11-12th Feb 2016







Numerical Precision testing

How gracefully does the algorithm degrade with limited precision?

Double vs single

```
%% Now try fixed point
L = pow2(9); % length of windows
alpha = 2.56; % value from Gianni
W = chebwin(L, 20*alpha);
sW = single(W); % convert offline designed va
fW = fi(W,1,8); % convert to fixed pt
N = pow2(7);
```

single Magnitude (dB) -20 double -150 0.1 0.2 0 0.3 0.4 0.5 Normalised frequency [cyles/s] 10 error (single-double) 10⁻⁵ 10-10 0.1 0.2 0.3 0.5 0 0.4 Normalised frequency [cyles/s]

Length of window = 2^{12} , dB (sidelobe) = -51.20

Amplitude of weight 0.6 0.7

0

1000

500

1500

2000

2500 sample #, (length N = 4096)

3000 3500 4000 4500



Computing for SKA 11-12th Feb 2016

freqz(single(fW),1,N)

Numerical Precision testing

Fixed point simulations: Requires care & iterative design





Comparison of single & fixed point

- 1. Double "Golden model"
- 2. Single (good for testing)
- 3. Fixed point (various)

Issues with:

• Saturation, RFI flagging



CENTRAL SIGNAL PROCESSO

Our models

- Easy to spawn variants
 - Add "convert" blocks early
 - Propagate types
- Easy to concatenate models
 - ICDs hardly necessary
- Convenient for block processing
 - But hard for exception handling



IP spinoffs

- Taylor the "FFT"
 - faster, more efficient ... but ...
- Fixed pt & shorten the FPGA development
- Develop our local capability
- Thermal modelling





Models demonstrate/validate the algorithm

- Assist with hardware programming/debugging
- Allows scenario testing
- "Golden model" encapsulates unambiguously the algorithm

But

Many FPGA issues not modelled

Corner turners, memory limitations, IP blocks



