SDP Compute for 50 Years - an awareness

C4SKA at AUT
2017-02-09

tn@compucon.co.nz (personal opinion)
Outline

- Costs of SKA1 in Euro
  - Design and Construction ~ 1B
  - Operating = 115M * 50 years
  - Electricity ~ 8%
  - SKA2 budget ~ 10 times?

- Challenges on SDP
  - Wave after wave of revamping
  - 9 Overviews
  - 1 Philosophical View- not that!

Image Credit
https://thenounproject.com/term/old-man/191197/
SKA Process Overview

Image credit: SDP Consortium Update 2016-06-21 Jeremy Cole page 12
SDP Science Objectives Overview

- System Sizing paper (SDP-038, Cambridge, 2016-0721)
  - Assumed 25% hardware utilisation efficiency (remember this)
  - Not based on peak computational capacity requirements
SDP Design Overview

(not to scale)

- Architecture
- QA
- AT
- MT
- Architecture
- Integration Prototyped

- Software
- Hardware

- Tender & Contract
- Construct

2017-02-09

2018-03-31
SDP Algorithm Overview

Continuum Imaging most demanding & reduction process is iceberg of the tip below

- **Algorithm AI (dataset size dependent)**
  - Gridding: \( Nk^2 > 100 \)
  - FFT: \( 5/32 \log_2 N < 5 \)
  - Cleaning ?

- **x86 Hardware AI (fixed)**
  - CPU < 5
  - Xeon Phi ~ 5
  - GPU > 25

- **Challenge**
  - Assumption of 25% HWU?
SDP Hierarchy Overview
Prescribed by Execution Framework SDP-015

- System Hierarchy
  - X compute islands
  - master node + data buffer + Y compute nodes
  - Same for LOW & MID

Source: SDP-018 Data Processor Platform (ASTRON 2016-0715)
Hardware Parameters Overview
Meet $, wattage, HWU, AI

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Table 4 on AI attainable on # GPU
Assume GPU capable of 1TB/s implying 5.5PB/s LOW 5.8PB/s MID

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- Hardware Sizing Guidance
  - 1TB/s
  - 5TFLOPS SP
  - AI = 5
  - 25% HWU
  - ~500W
  - >5000 nodes @
Technology Trend Overview

1965 – 2015 Moore’s Law
Cost per transistor has been on a linear decline during Moore’s Period

2015 – 2030 Moore’s Wall
Reaching physical limits
Trends and Challenges in Big Data, Ion Stoica, UC Berkeley, PDSW-DISCS 16, slide 43
Near Term Technology

- **CPU**
  - 25% performance improvements
  - Mostly by increasing number of cores, SOC and SIP (such as EMIB)

- **Memory**
  - 35 per year
  - Stacked technologies
  - Attain 1TB/s in 2017 (AMD Vega HBM2)

- **Network**
  - 40% per year
  - 100/200/400GbE NIC on horizon
Long Term Technology

- 2017 – 2030 Evolutionary
  - Software catching up on hardware
  - Allows expansion of science objectives
  - SKA2 on scope, dynamic range & resolution

- 2030 – 2070 Revolutionary
  - New programming model
  - FPGA
  - Quantum
  - Memory Processing

- Immediate Thought
  - Sub-arraying is a good idea
New Zealand 50 Years

- Views for SDP
  - High or Low language abstraction?
  - Open or Closed SW standards?
  - More emphasis on HW knowledge

- NZ well positioned
  - Contribute to SKA
  - Spin off via academic-industry collaboration projects
    - Collate range of expertise
    - Promote open architecture

Being aware of situation