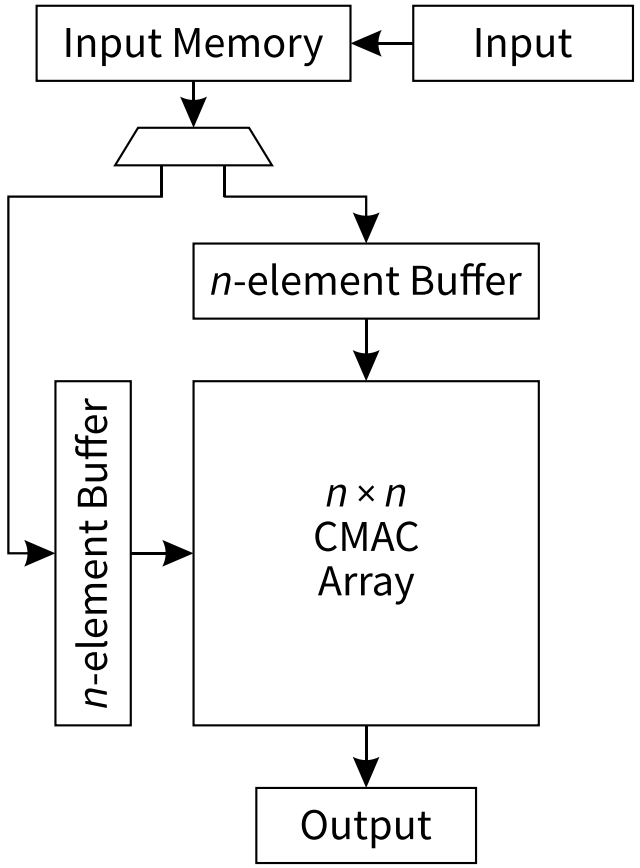
MASSEY UNIVERSITY

Multiple-accumulator CMACs and FX correlator efficiency

Stepan Lapshev

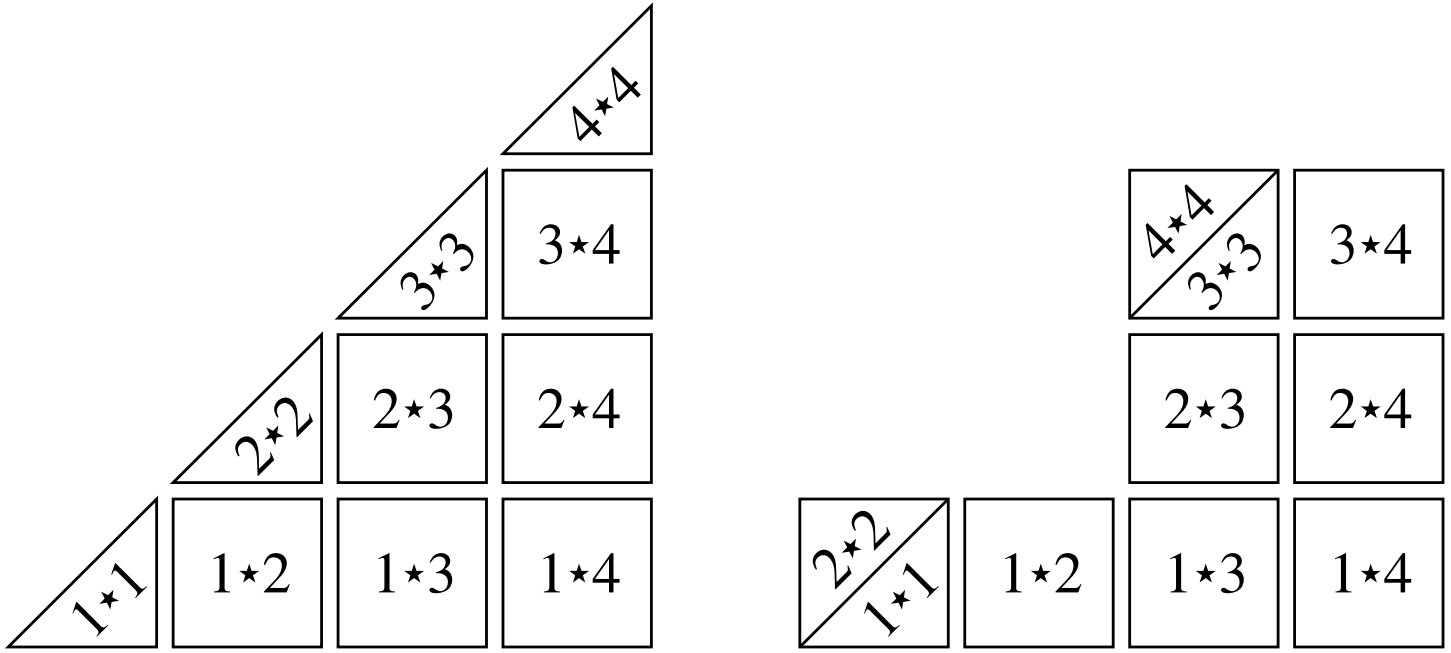
Supervisor: Dr Rezaul Hasan

Original FX architecture



- The on-chip memory stores data samples for all 2*N* signals for a portion of frequency channels
- Input signals are split into *w* sets of *n* signals for CMAC processing
- Two sets of *n* signals are correlated with each CMAC operation
- One accumulation produced by the CMAC array is called a sub-integration (SI)

Pattern of SIs



Architecture pros/cons

Advantages:

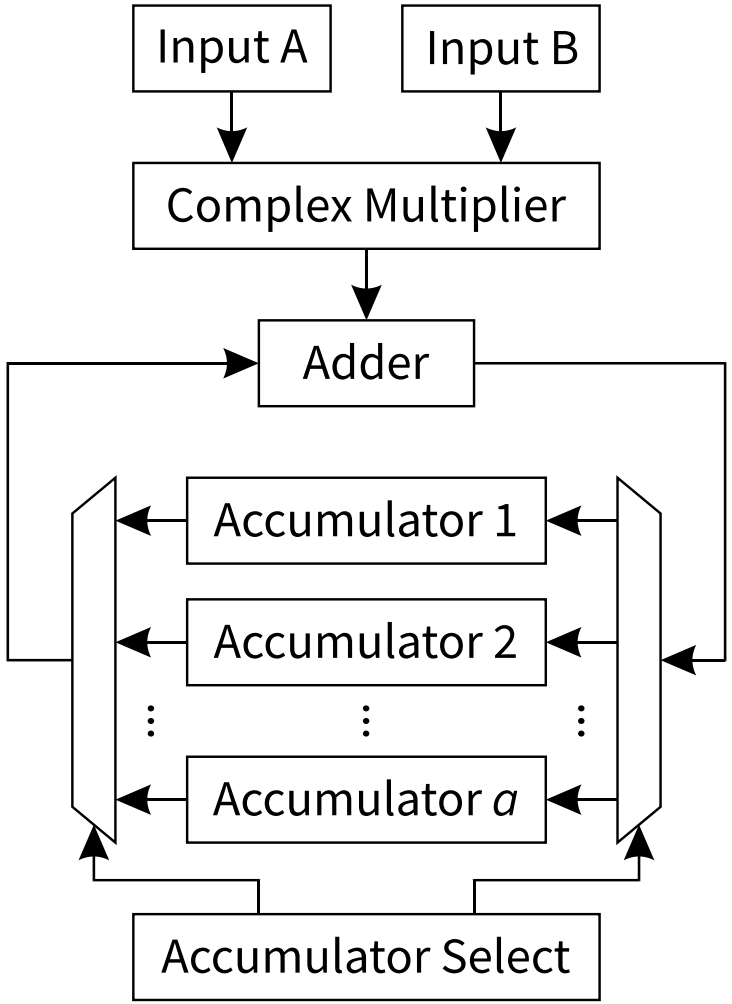
- Every sample is delivered to only one processing chip
- Flexible with respect to *N* and the bandwidth
- Scales easily
- Can be made using standard technologies

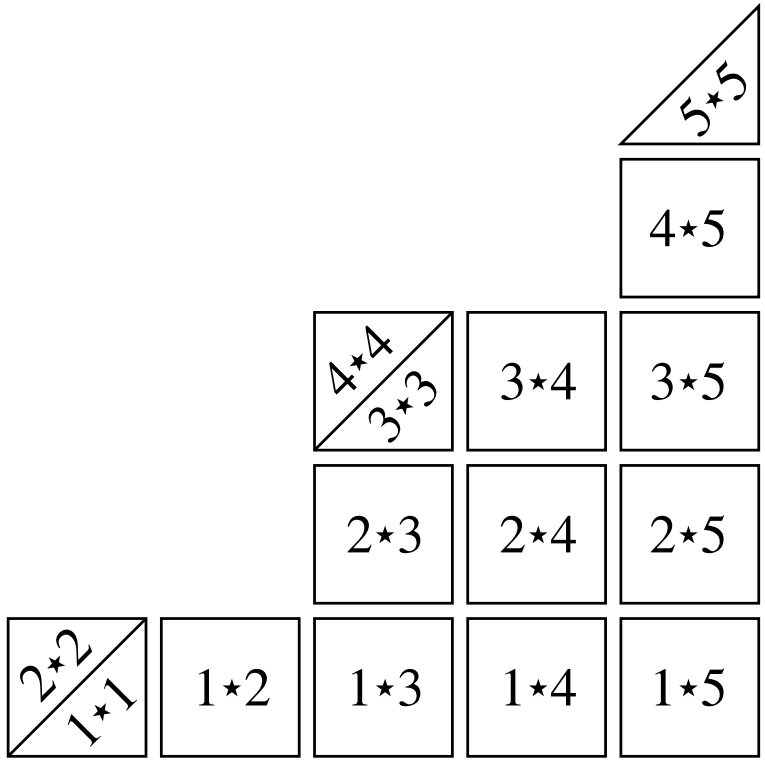
Disadvantages:

- Every data sample is read *w* times from the memory because it is used in *w* SIs
- Often a memory-limited design: 2 memory operations per 1 CMAC operation

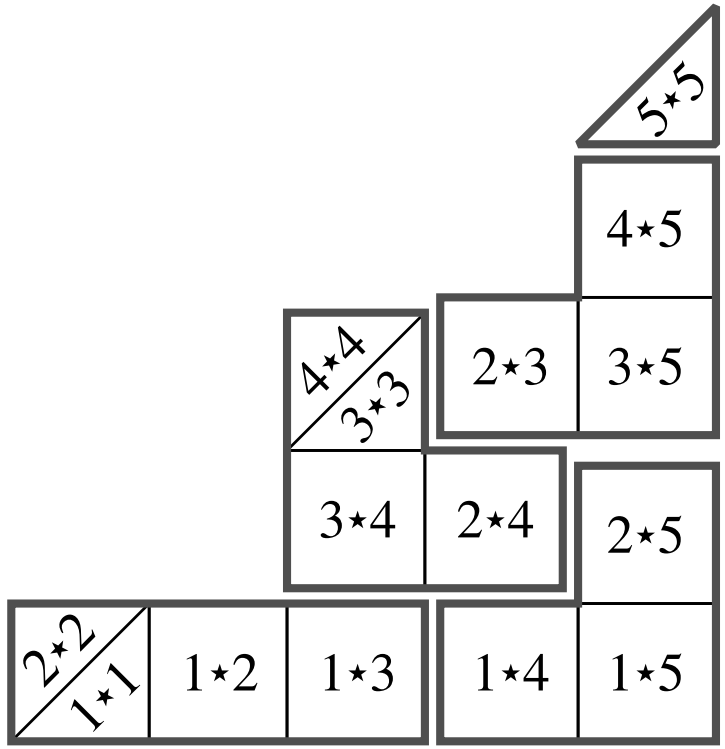
Improvement: Multiple-accumulator CMACs

- Use CMACs with $a > 1$ accumulators
- Group SIs that share input signals into groups of a
- When processed in correct sequence, this allows to reuse data samples currently in the processing buffer
- This significantly reduces the number of memory operations for the same number of CMAC operations, the same input and the same output


Input A
Input B
Complex Multiplier
Adder
Accumulator 1
Accumulator 2
Accumulator a
Accumulator Select


5⋆5
4⋆5
4⋆4
3⋆3
3⋆4
3⋆5
2⋆3
2⋆4
2⋆5
2⋆2
1⋆1
1⋆2
1⋆3
1⋆4
1⋆5

$w = 5, a = 1$


5⋆5
4⋆5
4⋆4
3⋆3
2⋆3
3⋆5
3⋆4
2⋆4
2⋆5
2⋆2
1⋆1
1⋆2
1⋆3
1⋆4
1⋆5

$w = 5, a = 3$

Reduction in memory quantified: Number of read operations *R*

$$R(a,w) = (a+1)\,A + (B+1)\,\operatorname{sgn} B - \left\lfloor \frac{w}{2} \right\rfloor \operatorname{sgn}(a-1) + (w \bmod 2)\,(1 - \operatorname{sgn} B)\,,$$

where

$$A = \left\lfloor \frac{\lfloor w^2/2 \rfloor}{a} \right\rfloor$$

and

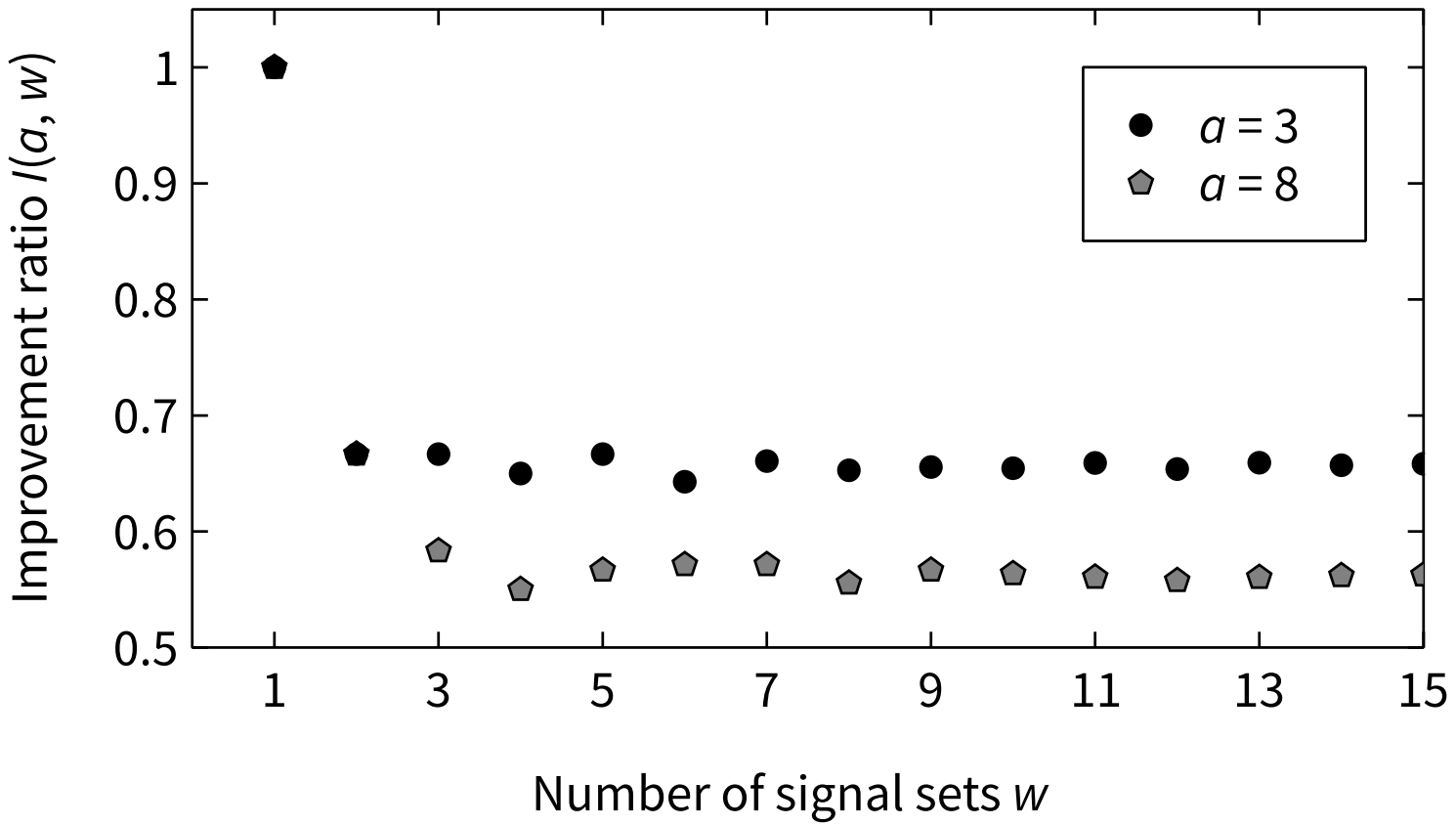
$$B = \left\lfloor \frac{w^2}{2} \right\rfloor \bmod a\,.$$

Reduction in memory quantified: Improvement ratio *I*

$$I(a, w) = \frac{R(a, w) + w}{w^2 + w}$$

$$I \simeq \frac{a + 1}{2a}$$

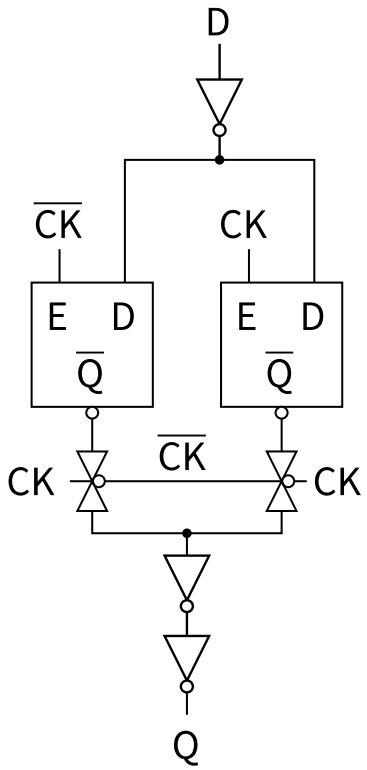
Reduction in memory quantified



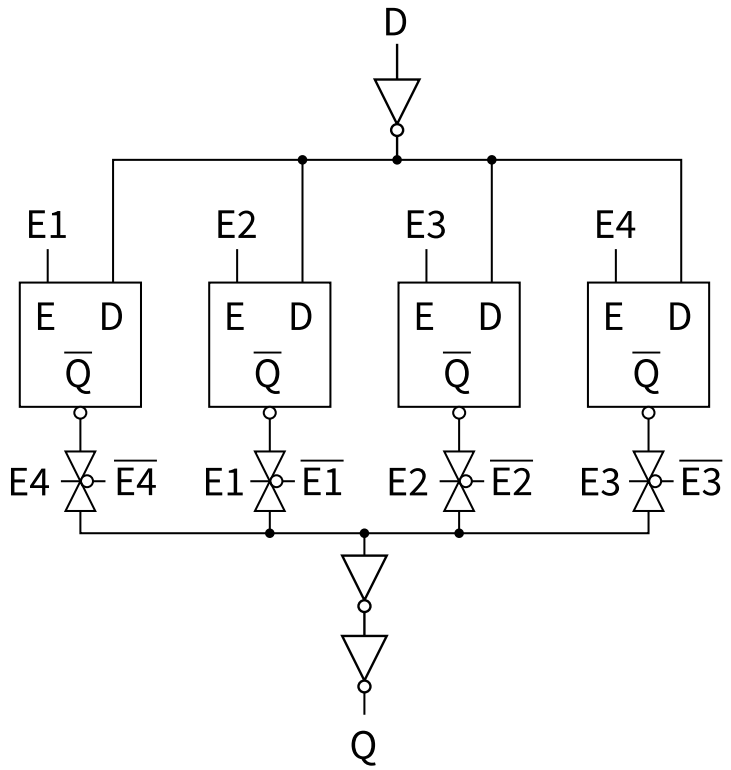
Hardware implementation

- Implementation of 8-bit CMACs in a high-performance 28 nm CMOS process
- Custom design of equivalent $a = 1$ and $a = 3$ designs to evaluate advantage of the multiple-accumulator approach
- Important to find out that memory savings are not overwhelmed by any increase elsewhere

Accumulator storage cell design



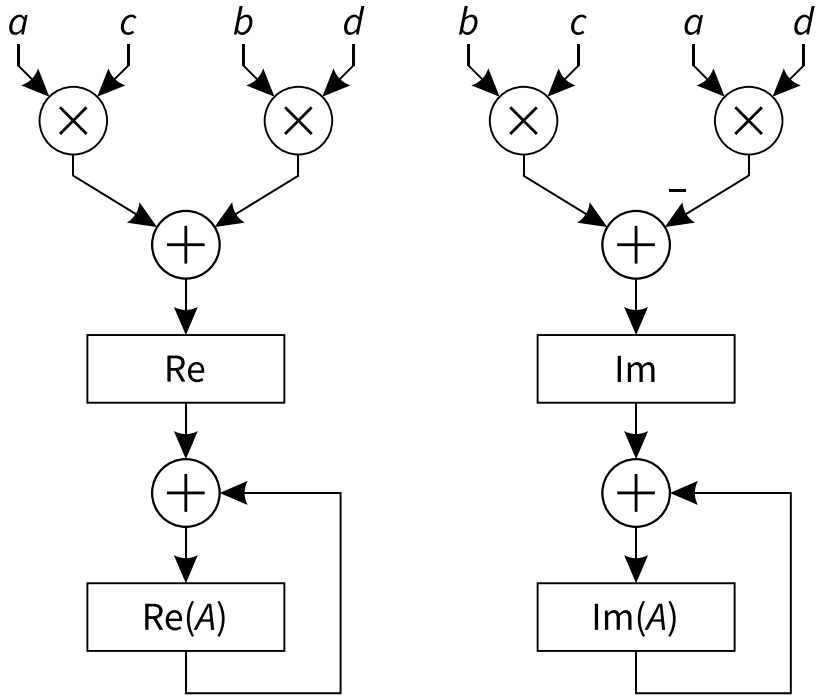
$a = 1$



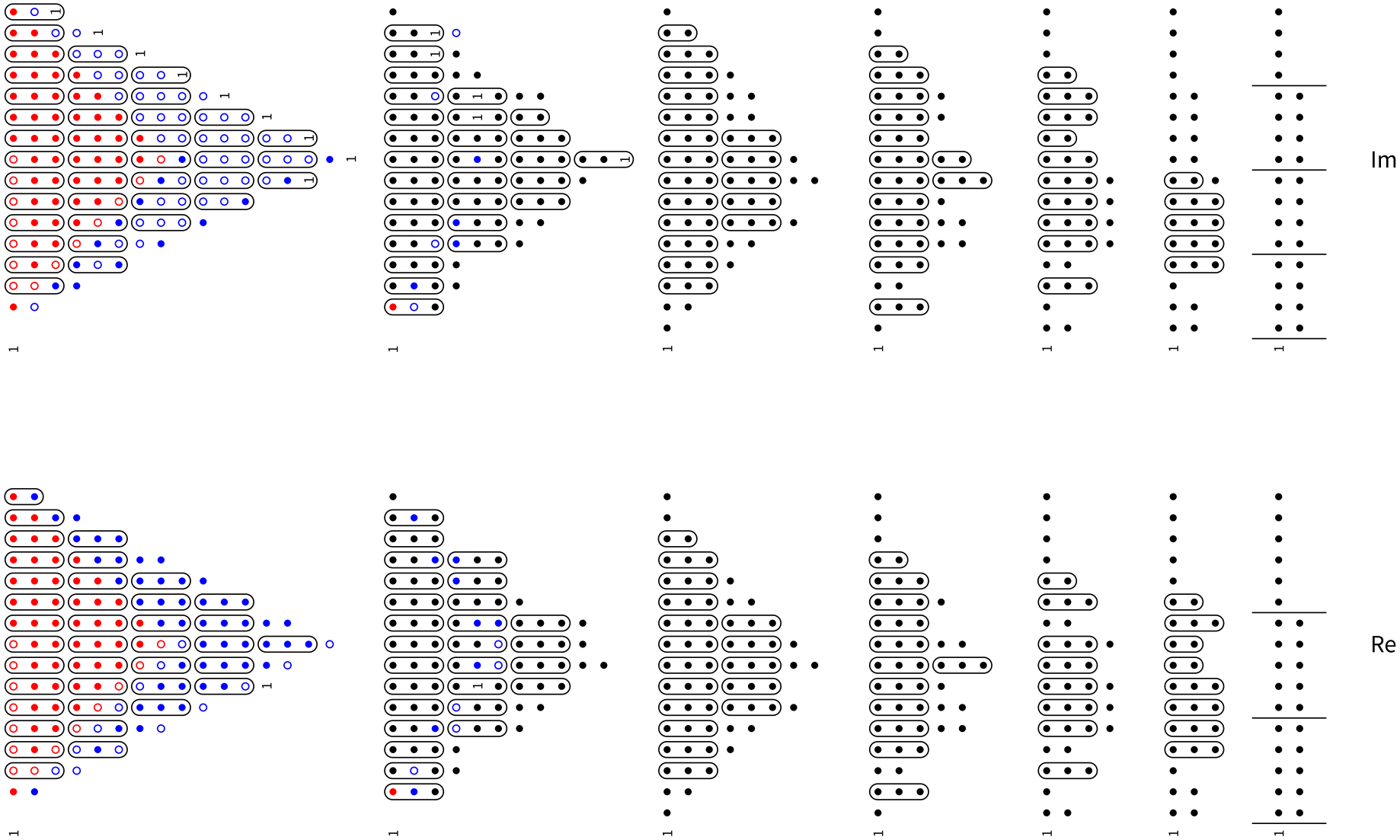
$a = 3$

CMAC design

Correlation: $(a + ib)(c - id)$



- Two-stage pipeline: multiplication and accumulation
- Fused multiplier design based on logarithmic reduction adder trees: highest efficiency in terms of energy per operation and circuit delay
- Soft-edge flip-flops between stages to increase timing performance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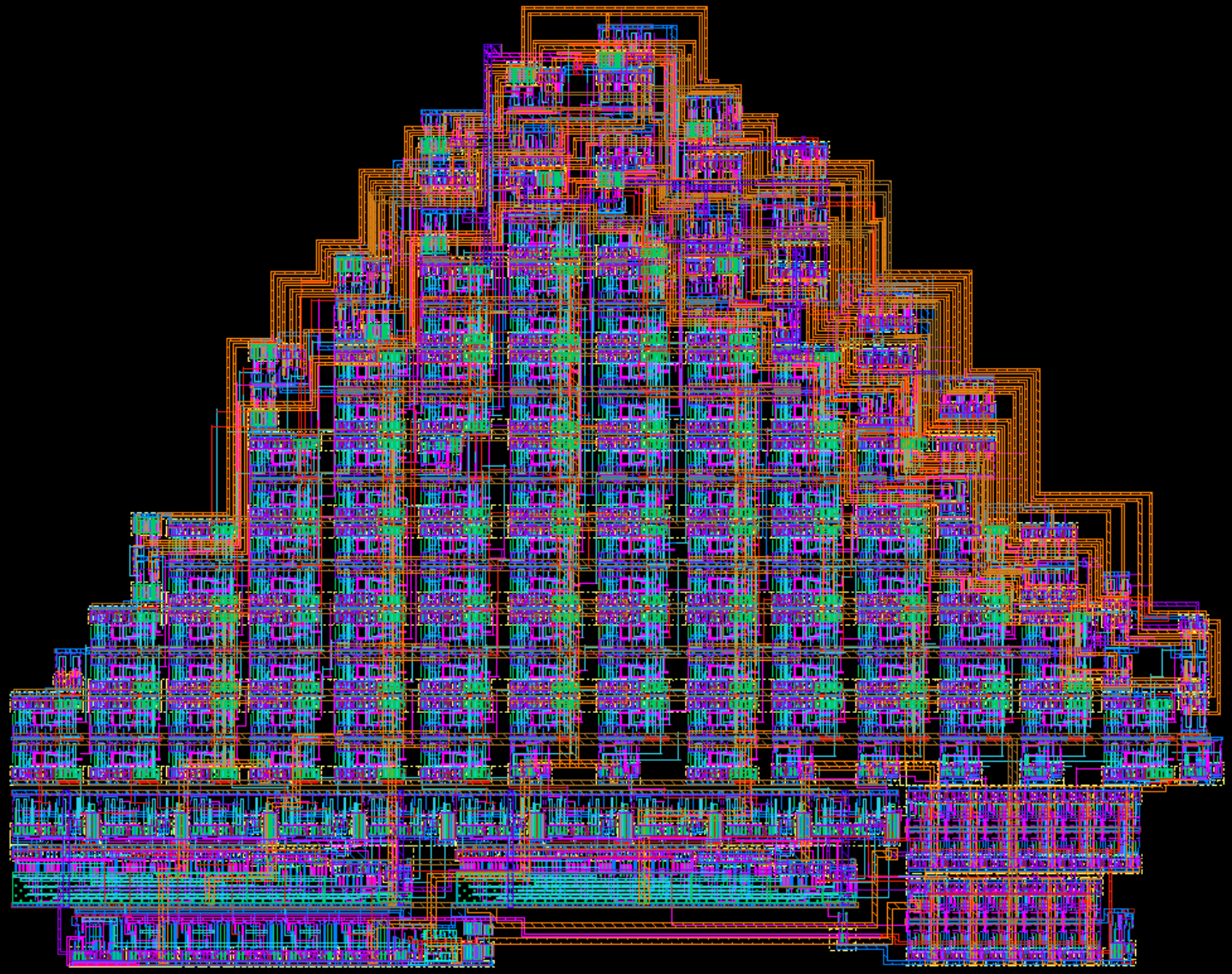

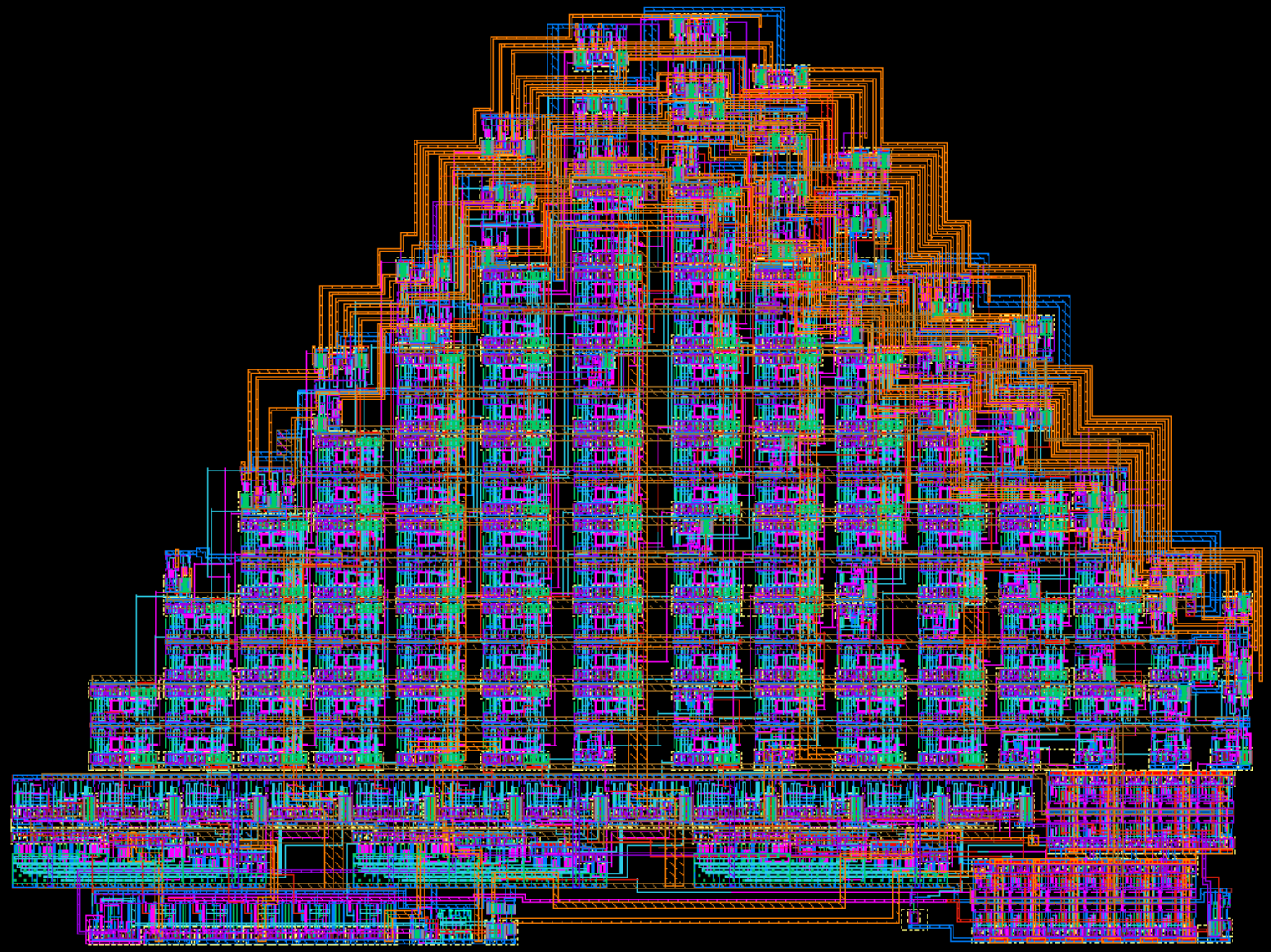

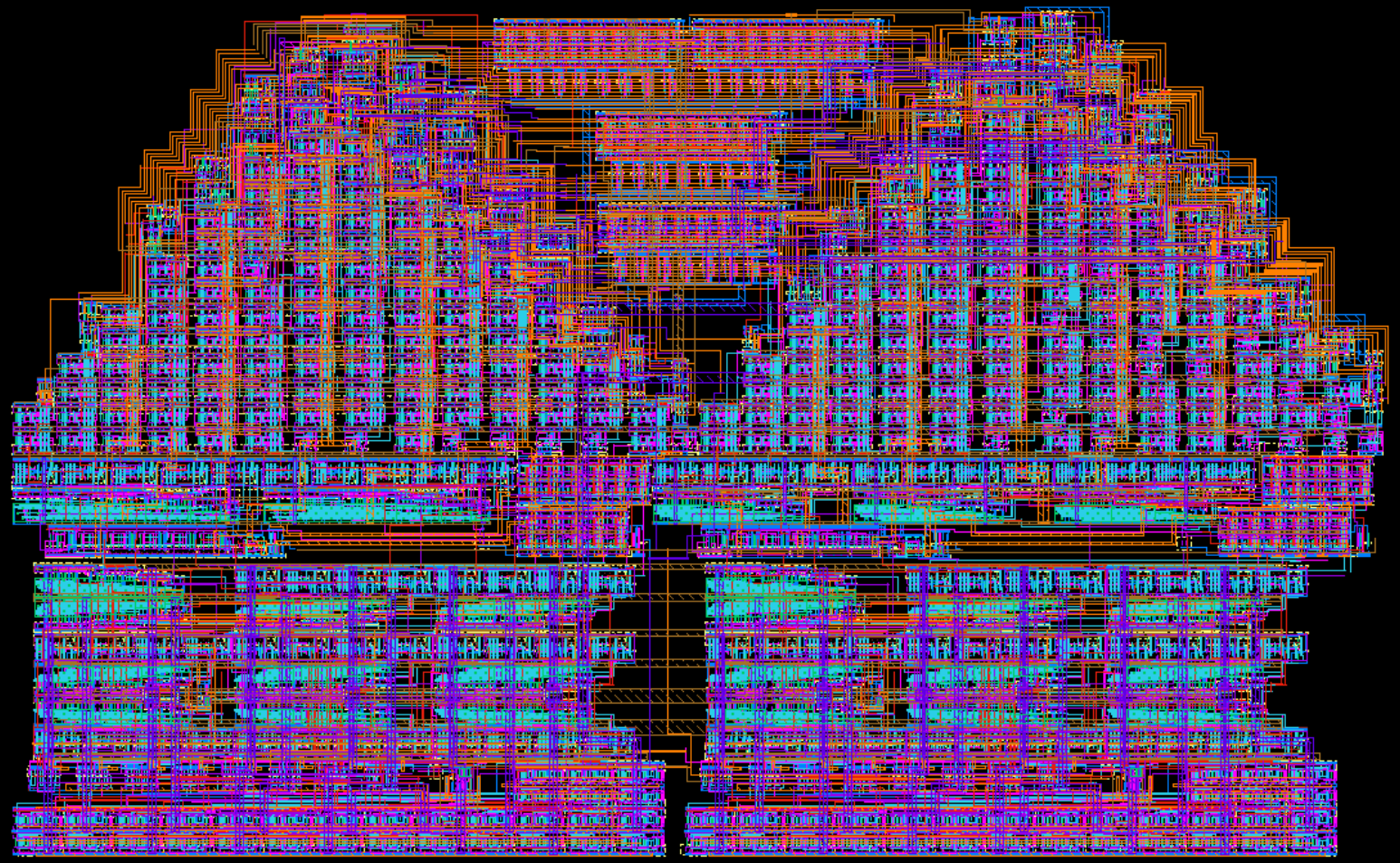

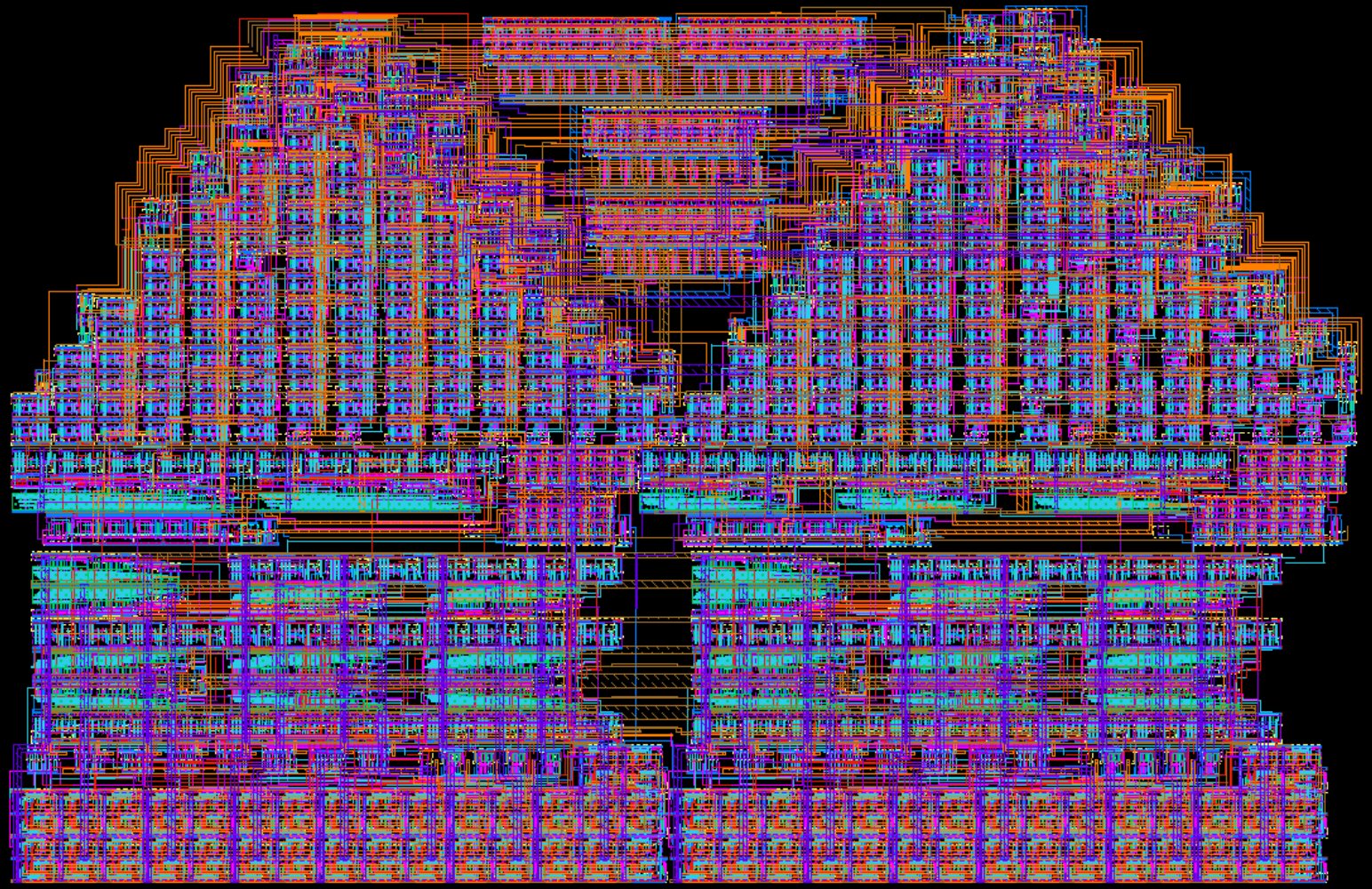

Simulation results

Parameter or Metric	Value	
Temperature, °C	60	
Cycle time, ns	0.8	
Accumulator count *a*	1	3
Total energy/op, pJ	2.614	2.578
Multiplier energy/op, pJ	1.619	1.373
Accumulator energy/op, pJ	0.995	1.205
Total leakage, µA	228.8	243.1
Accumulator leakage, µA	60.3	74.6
Circuit area, μm^2	3950.2	4160.6