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MULTIPLIER-FREE FPGA LUT IMPLEMENTATION OF RADIO-ASTRONOMICAL SIGNAL PROCESSING USING DISTRIBUTED ARITHMETIC & MASSEY SCIENCE SPINOFFS IN SKA RELATED Ph.D. PROJECTS

Presented by: Rezaul Hasan, Ph.D. (UCLA), Director

Center for Research in Analog and VLSI microsystem dEsign (CRAVE), School of Engineering and Advanced Technology, Massey University Auckland 0632, New Zealand

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DISTRIBUTED ARITHMETIC

- Well-known method to save resource in MAC structures
- Trades memory with combinatorial computation logic
- Ideal to implement DSP in LUT based FPGA
- Original paper by Peled and Liu (Princeton EE) in IEEE Transactions on Acoustics, speech and signal processing, “A new hardware realization of digital filters”
- Allows novel exploitation of the symmetry and periodicity of DFT/DCT coefficients in minimizing hardware
- Maybe suitable for very high speed BIG-DATA applications

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UNDERLYING ALGORITHM OF DISTRIBUTED ARITHMETIC

Most signal processing/ Astronomical signal processing ends-up being a collection of sum-of-products of coefficients (often with exploitable symmetry and periodicity) and signal data. For example, the output quantity, *Y* being given by the discrete-time digital representation over time *T* as:

$$Y = A_0 \times X_0 + A_1 \times X_1 + A_2 \times X_2 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots + A_{T-1} \times X_{T-1}$$

Where *A* are coefficients and *X* are data-stream.

UNDERLYING ALGORITHM OF DISTRIBUTED ARITHMETIC

So that we can write,

$Y=\sum_{t=0}^{T-1} A_t \times X_t$

Using for simplicity, sign magnitude binary representation of the data X_t

$Y=\sum_{t=0}^{T-1} A_t \times [\sum_{b=0}^{N-1} X_{t,b} \times 2^b]$

Where, $X_{t,b}$ is the binary value at the b^{th} bit location of the data X_t . Next we can interchange the two summations and bring them in front, so that,

$Y= \sum_{b=0}^{N-1} [\sum_{t=0}^{T-1} A_t \times X_{t,b} \times 2^b]$

UNDERLYING ALGORITHM OF DISTRIBUTED ARITHMETIC

Now, we look at the values of the sum,

$\sum_{t=0}^{T-1} A_t \times X_{t,b} = f(b)$, say,

For $b=0$ position,

$f(0) = [A_0 \times X_{0,0} + A_1 \times X_{1,0} + A_2 \times X_{2,0} + \ldots\ldots + A_{T-1} \times X_{T-1,0}]$

For $b=1$ position,

$f(1) = [A_0 \times X_{0,1} + A_1 \times X_{1,1} + A_2 \times X_{2,1} + \ldots\ldots + A_{T-1} \times X_{T-1,1}]$

For $b=2$ position,

$f(2) = [A_0 \times X_{0,2} + A_1 \times X_{1,2} + A_2 \times X_{2,2} + \ldots\ldots + A_{T-1} \times X_{T-1,2}]$

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For *b=3* position,

$f(3) = [A_0 \times X_{0,3} + A_1 \times X_{1,3} + A_2 \times X_{2,3} + \ldots\ldots + A_{T-1} \times X_{T-1,3}]$

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For *b=N-1* position,

$f(N\text{-}1) = [A_0 \times X_{0,N-1} + A_1 \times X_{1,N-1} + A_2 \times X_{2,N-1} + \ldots\ldots + A_{T-1} \times X_{T-1,N-1}]$

So, *Y* can be found by just shifting (matter of wire connection) and adding the *f*'s.

$Y = f(0) \times 2^0 + f(1) \times 2^1 + f(2) \times 2^2 + \ldots\ldots\ldots\ldots\ldots + f(N\text{-}1) \times 2^{N-1}$

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But, each *f*(*b*) for each bit position can have at most 2^T distinct values which can be designated as *fval*(*0*), *fval*(*1*), *fval*(*2*),……*fval*(2^T-1). These distinct values can be pre-stored in FPGA mux-based LUTs, and, selected for each *f*(*b*) by using the address:

A(b): [$X_{0,b}$ $X_{1,b}$ $X_{2,b}$ $X_{3,b}$ …….. $X_{T-1,b}$] into a [2^T *:1*] Mux

STRATIX series FPGA have lot of adders and lookup tables (memory + mux) that can implement distributed arithmetic.

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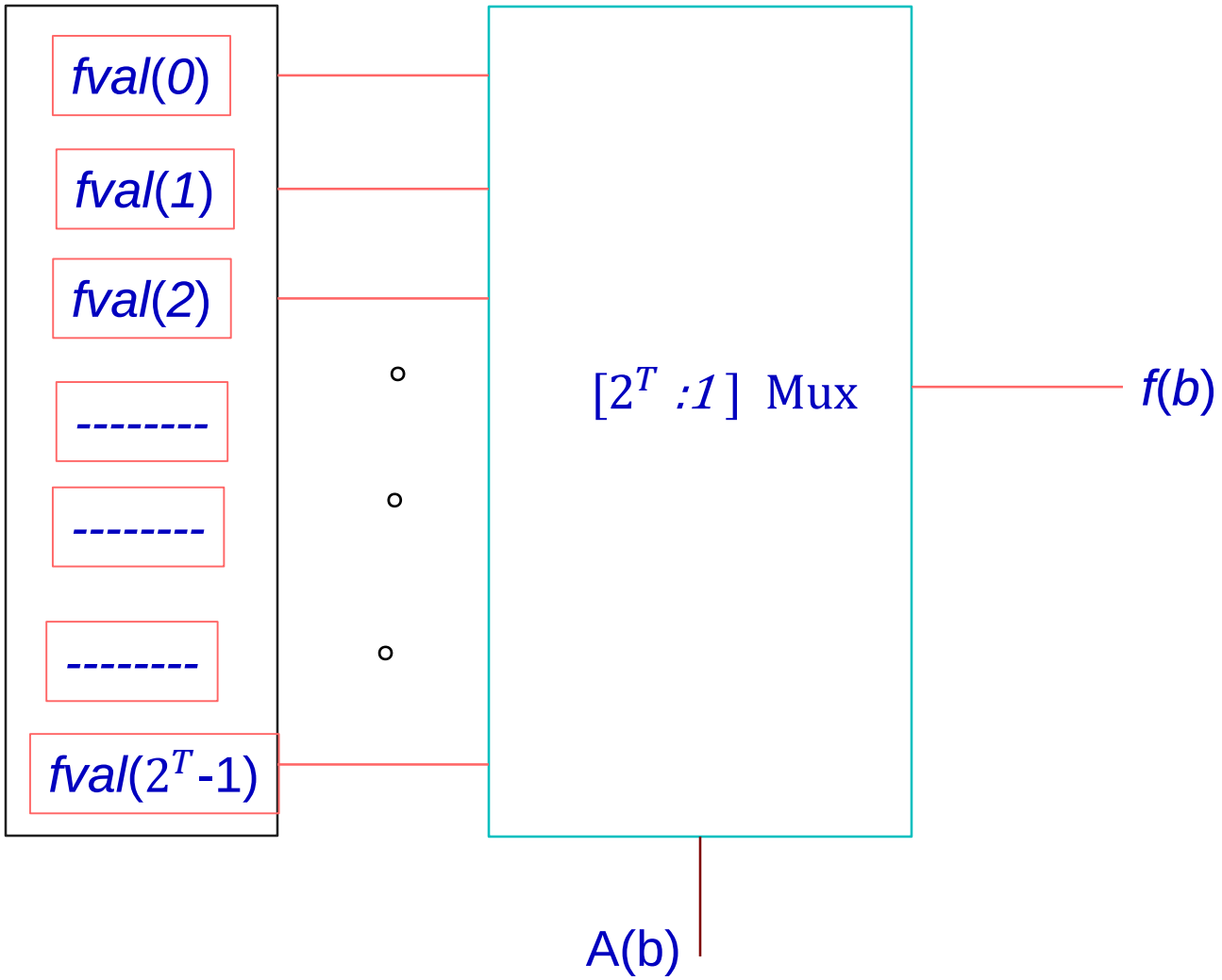
FPGA LUT IMPLEMENTATION



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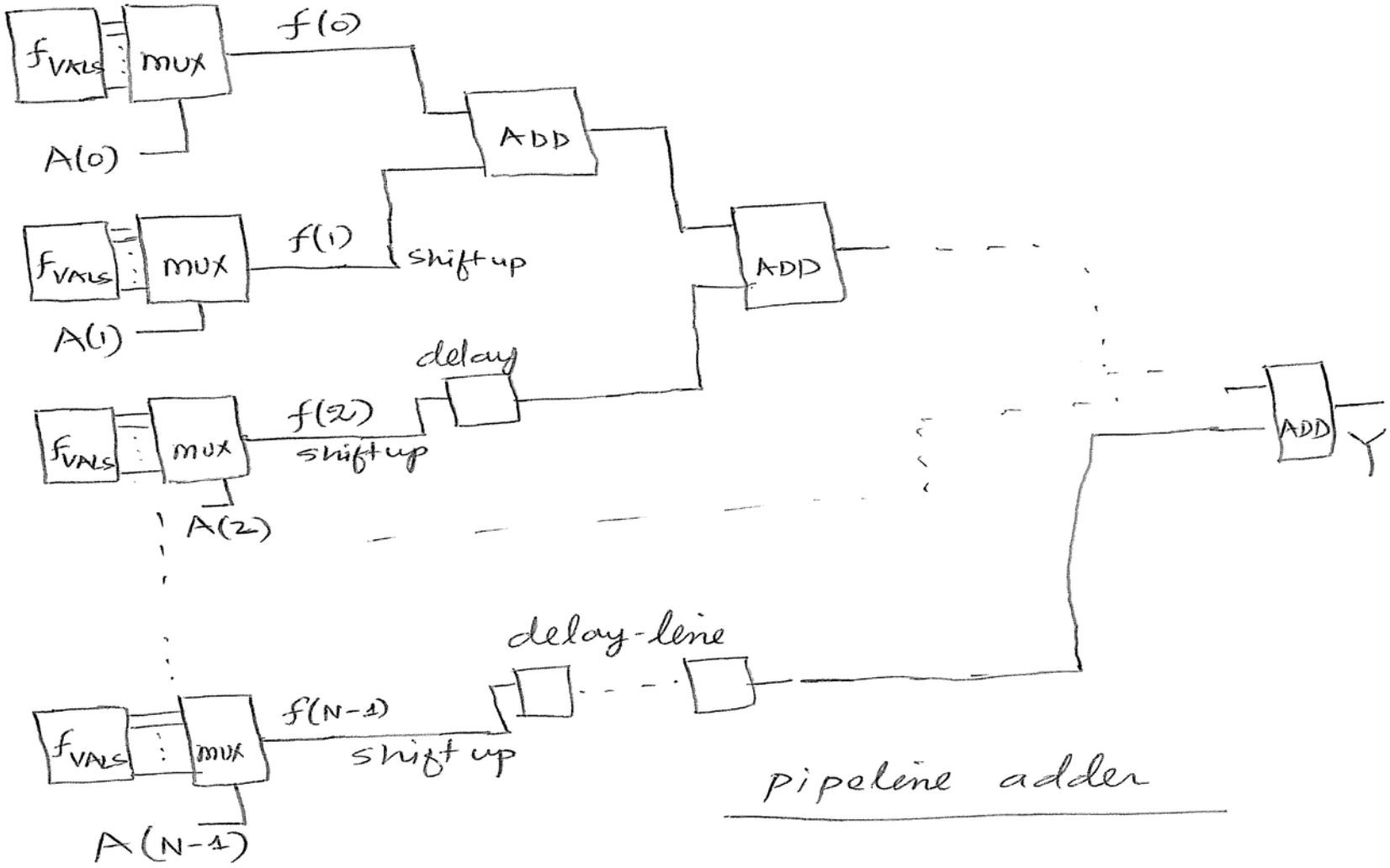
FPGA LUT PIPELINE IMPLEMENTATION



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MASSEY SCIENCE SPINOFFS IN SKA RELATED Ph.D. PROJECTS

COMPLETED PhD

Stepan Lapshev

PhD Thesis topic: CMOS VLSI Implementation of Very High Speed Correlator and Beamformer Circuit for Radio Astronomical Signal Processing (*Thesis submitted, awaiting oral exam*)

Peer-reviewed journal research article:

(1) Stepan Lapshev and S. M. Rezaul Hasan, "On the architecture for the X part of a very large FX correlator using two-accumulator CMACs, " Experimental Astronomy, Springer, vol. 41, no. 1, pp. 259-270, 2016.

(2) Stepan Lapshev and S. M. Rezaul Hasan, "New Low Glitch and Low Power DET Flip-Flops Using Multiple C-Elements," IEEE Transactions On Circuits and Systems-I: Regular Papers, vol. 63, no. 10, pp. 1673-1681, Oct. 2016.

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(3) Stepan Lapshev and S. M. Rezaul Hasan, “Using Multiple-Accumulator CMACs to Improve Efficiency of the X Part of an Input-Buffered FX Correlator,” Experimental Astronomy, Springer, Vol. 43, no. 2, pp.177-187, 2017.

REPORT: SKA MEMO

(4) Stepan Lapshev and Rezaul Hasan, *ASIC Design for Time-Domain Beamforming*, SKA CSP Memo 0023, 2017.

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IN PROGRESS:
Vignesh Raja Balu
PhD Thesis topic: Novel Architecture of Digital Array Processing Unit for Correlation in Interferometers.

Peer-reviewed journal research article:
(5) V. R. Balu and S. M. Rezaul Hasan, “Computationally Minimized X-part for FX Correlator in Big-data Interferometers,” IEEE Access, vol. 5, pp. 25353-25364, 2017.

Some more to come in 2018……

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Thank You!