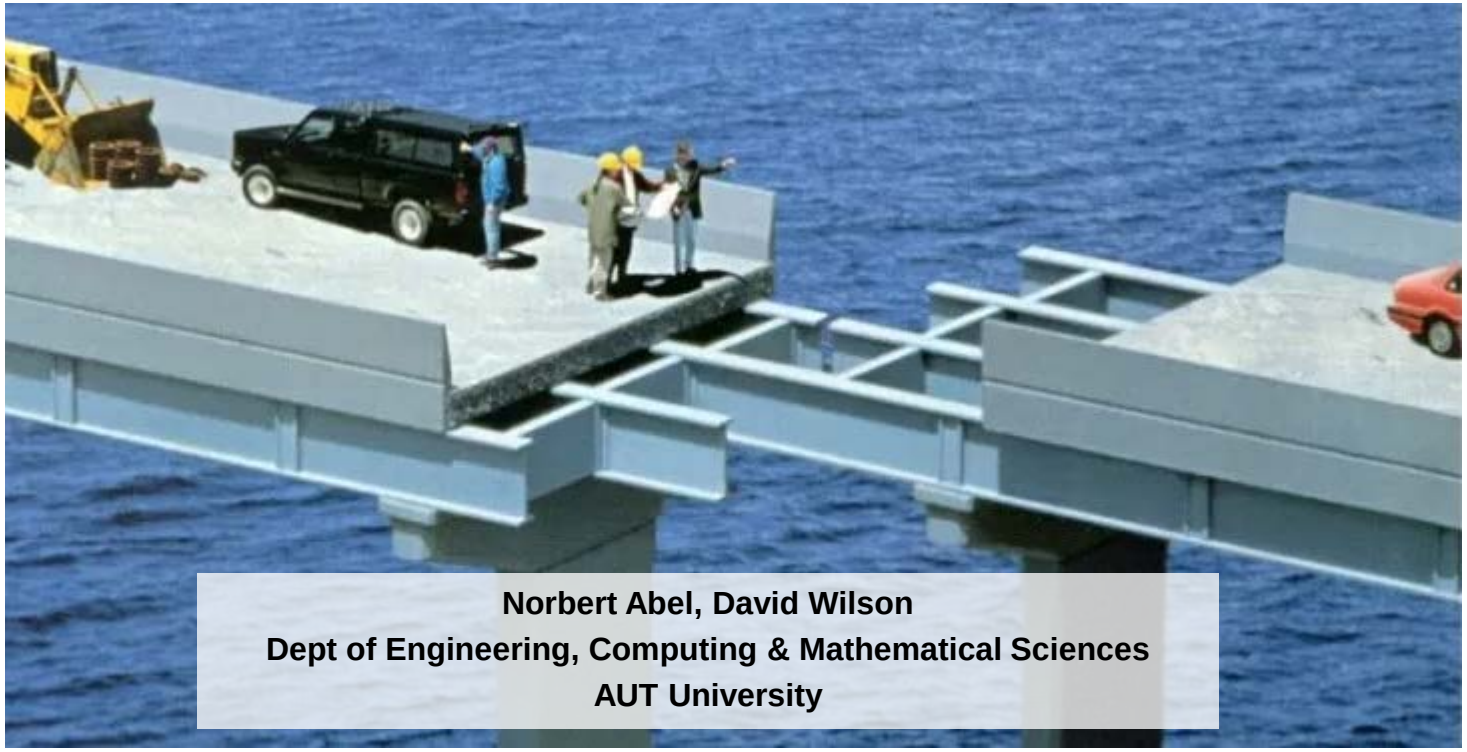
Bridging the gap between Matlab and FPGA code



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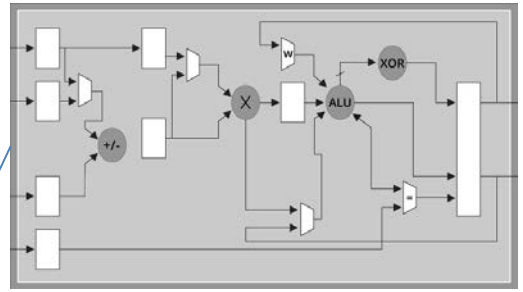
Dept of Engineering, Computing & Mathematical Sciences
AUT University

Matlab

```
for i=1:4
   omega    = (wv-wc)*t + wv*delayP(i) + rPhase;
   signal_t = exp(1j*(omega));
   s(i,1)   = sum(signal_t);
end
```

- ❑ Functional Verification
- ❑ Mathematical Precision
- ❑ Resource Consumption
- ❑ Performance



FPGA code

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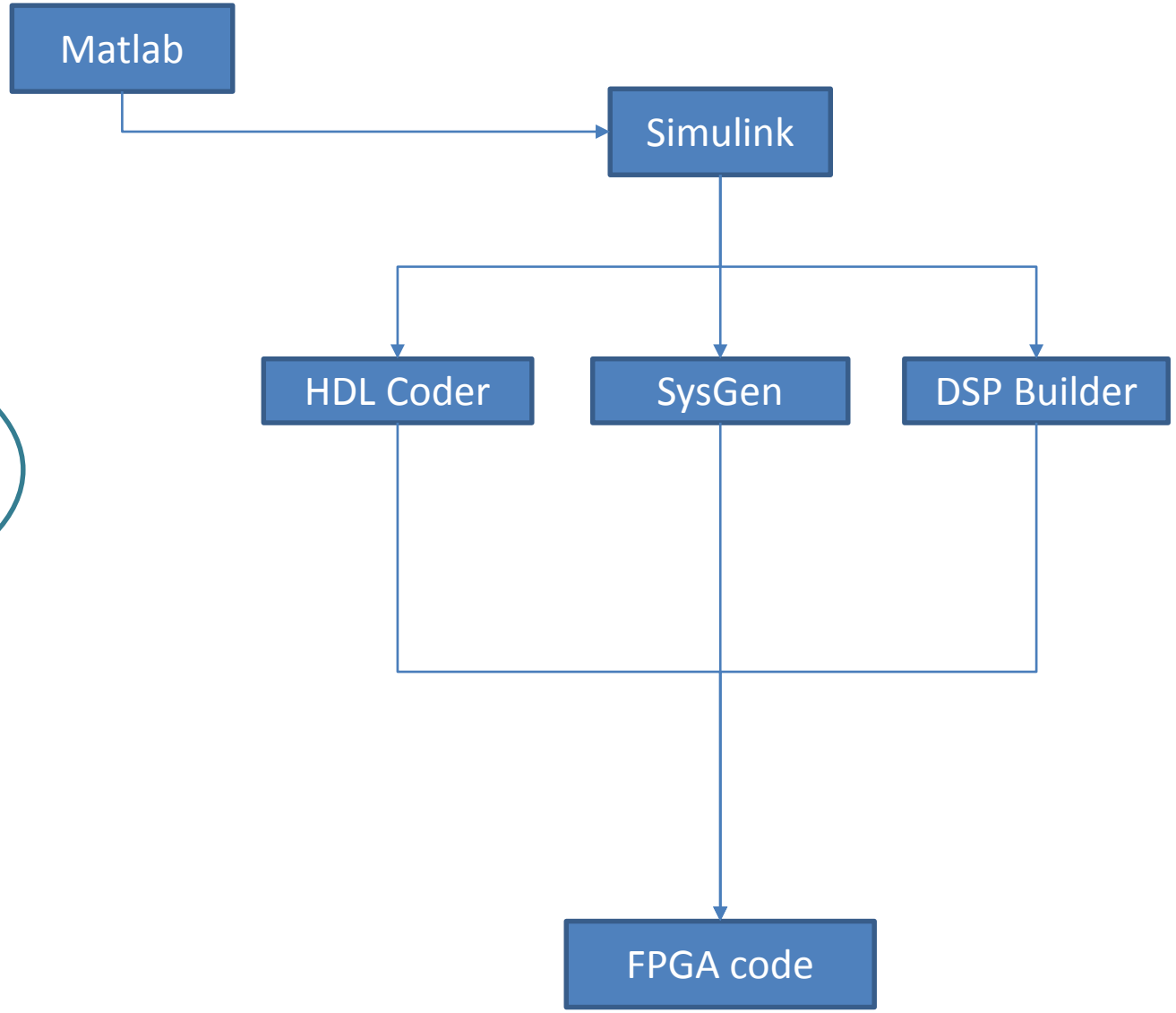


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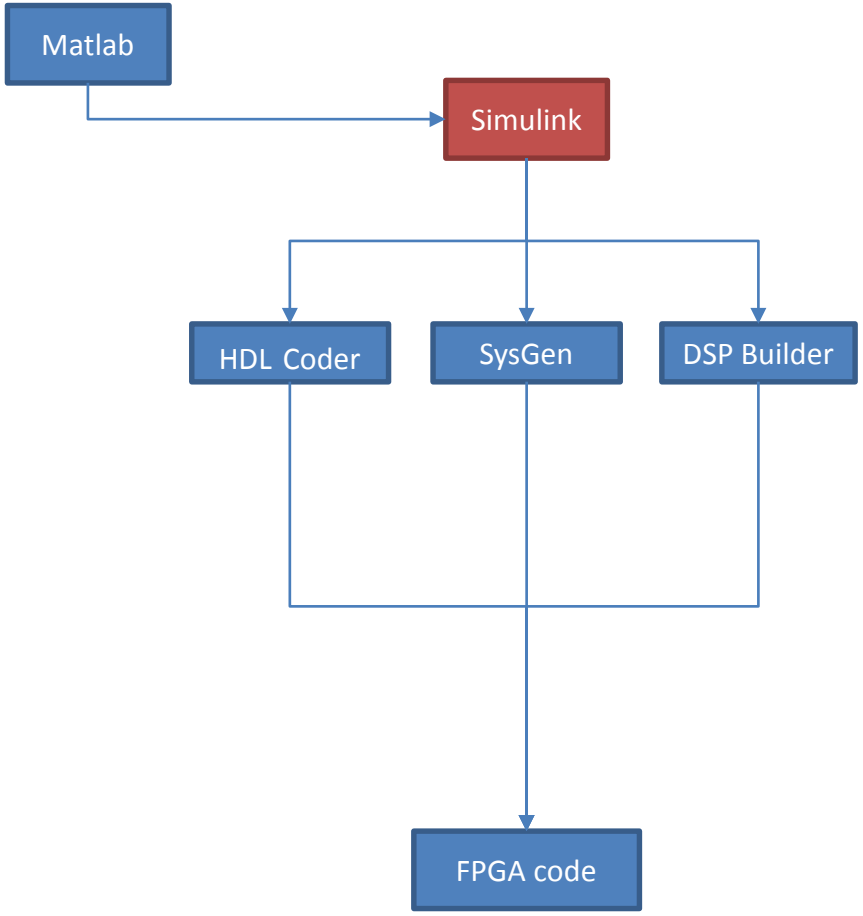
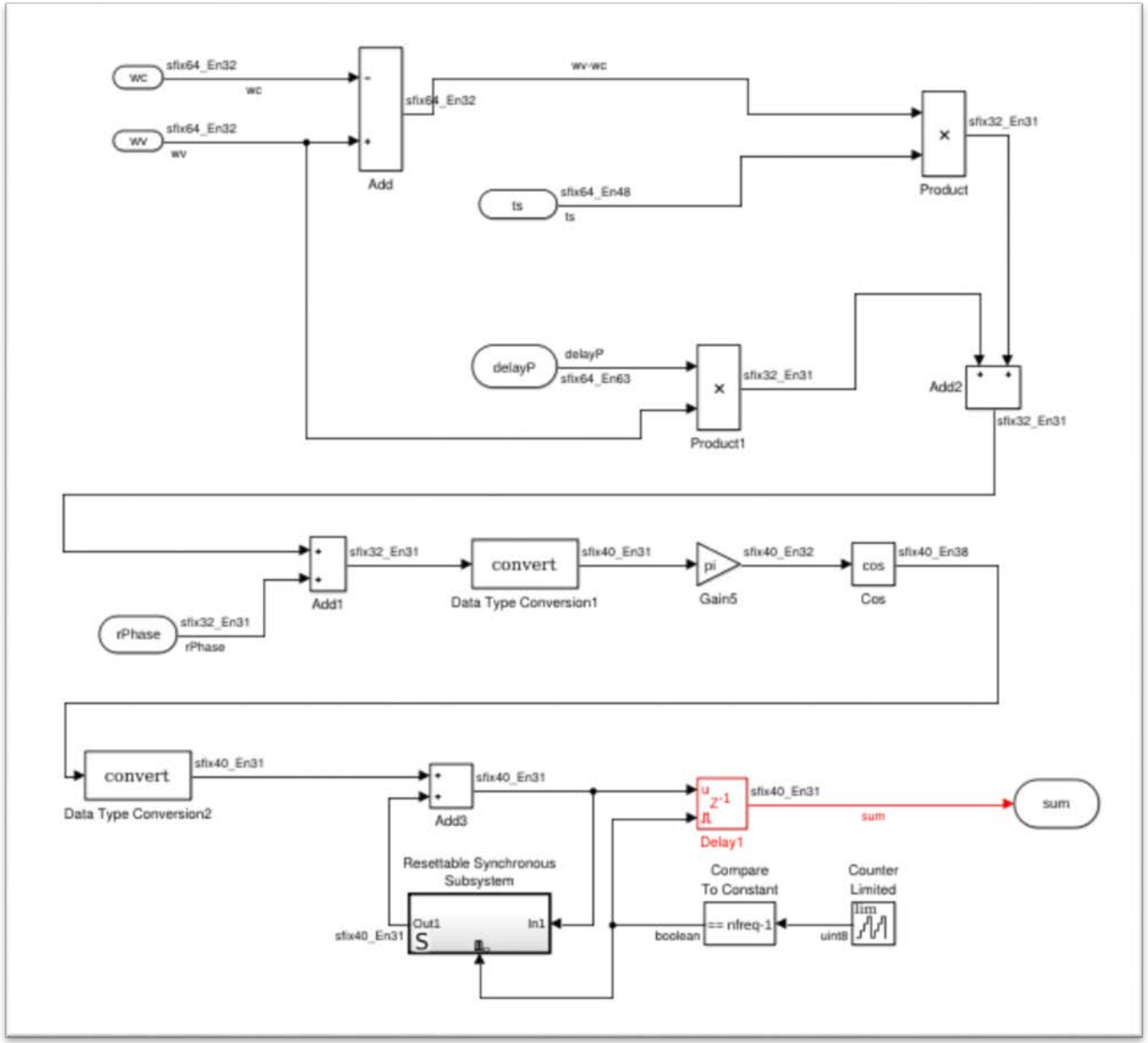
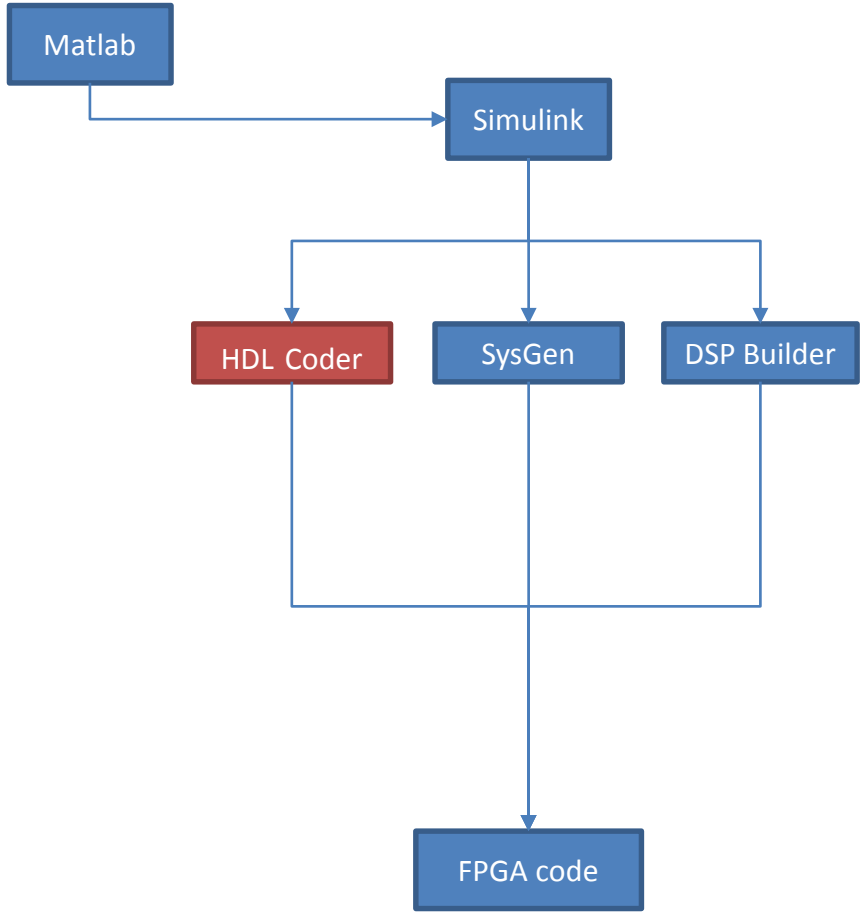



wc
sfix64_En32
wc
wv
sfix64_En32
wv
Add
sfix64_En32
wv·wc
ts
sfix64_En48
ts
Product
sfix32_En31
delayP
delayP
sfix64_En63
Product1
sfix32_En31
Add2
sfix32_En31
Add1
sfix32_En31
convert
sfix40_En31
Data Type Conversion1
pi
sfix40_En32
Gain5
cos
sfix40_En38
Cos
rPhase
sfix32_En31
rPhase
convert
sfix40_En31
Data Type Conversion2
Add3
sfix40_En31
Delay1
sfix40_En31
sum
sum
Resettable Synchronous Subsystem
Out1
In1
sfix40_En31
Compare To Constant
boolean
== nfreq-1
Counter Limited
uint8
lim


Matlab
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HDL Coder
SysGen
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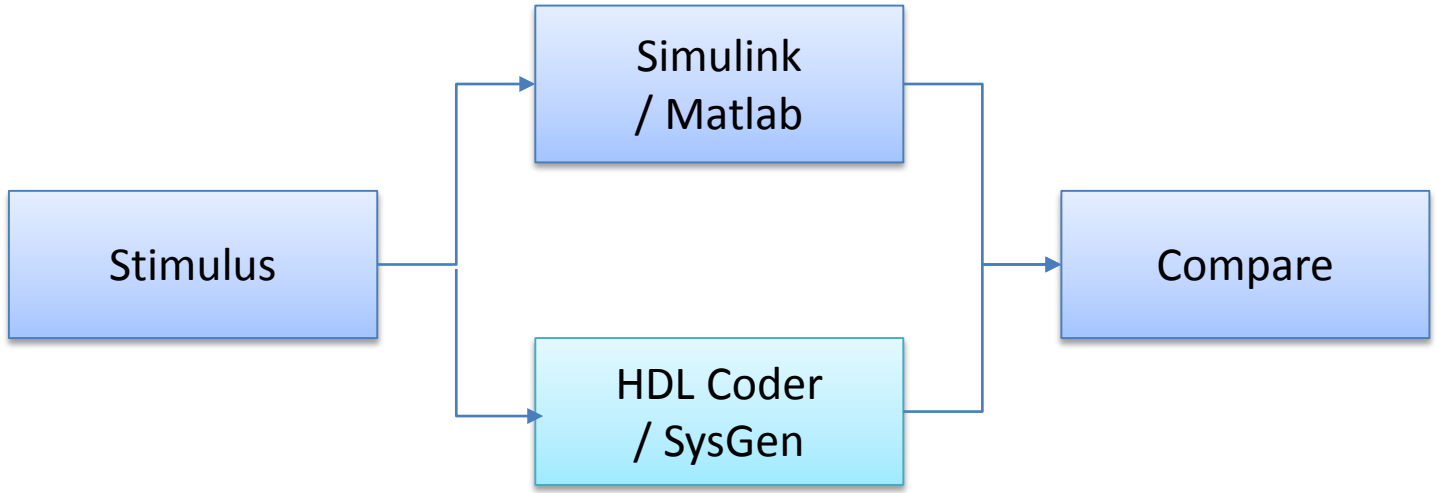
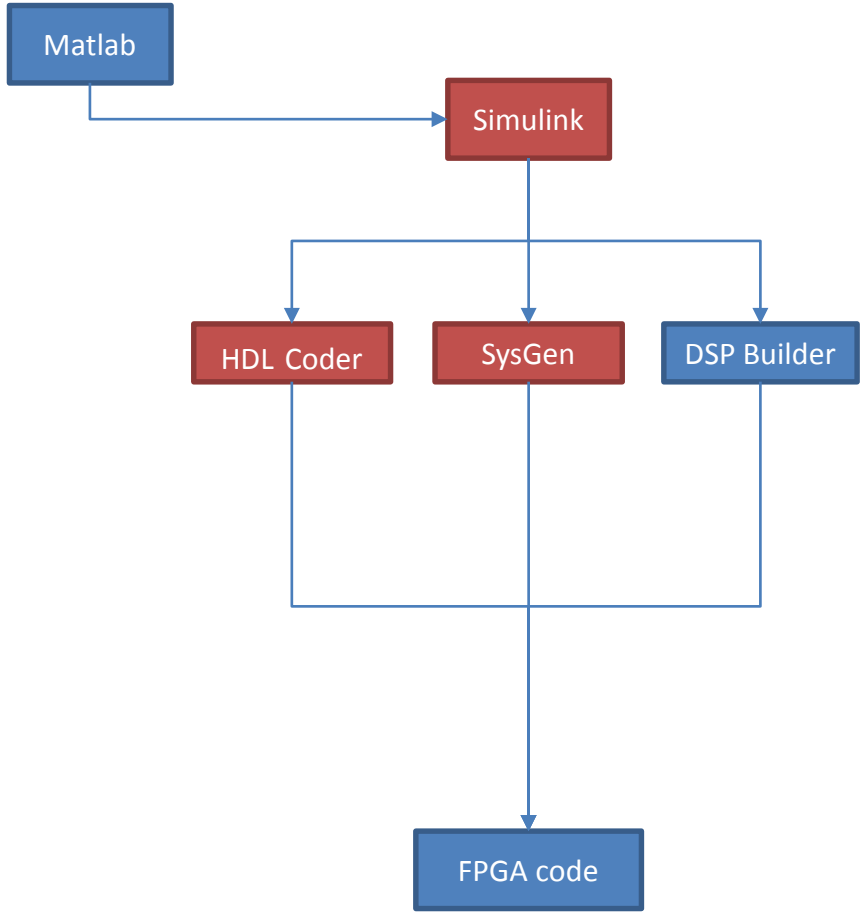
FPGA code





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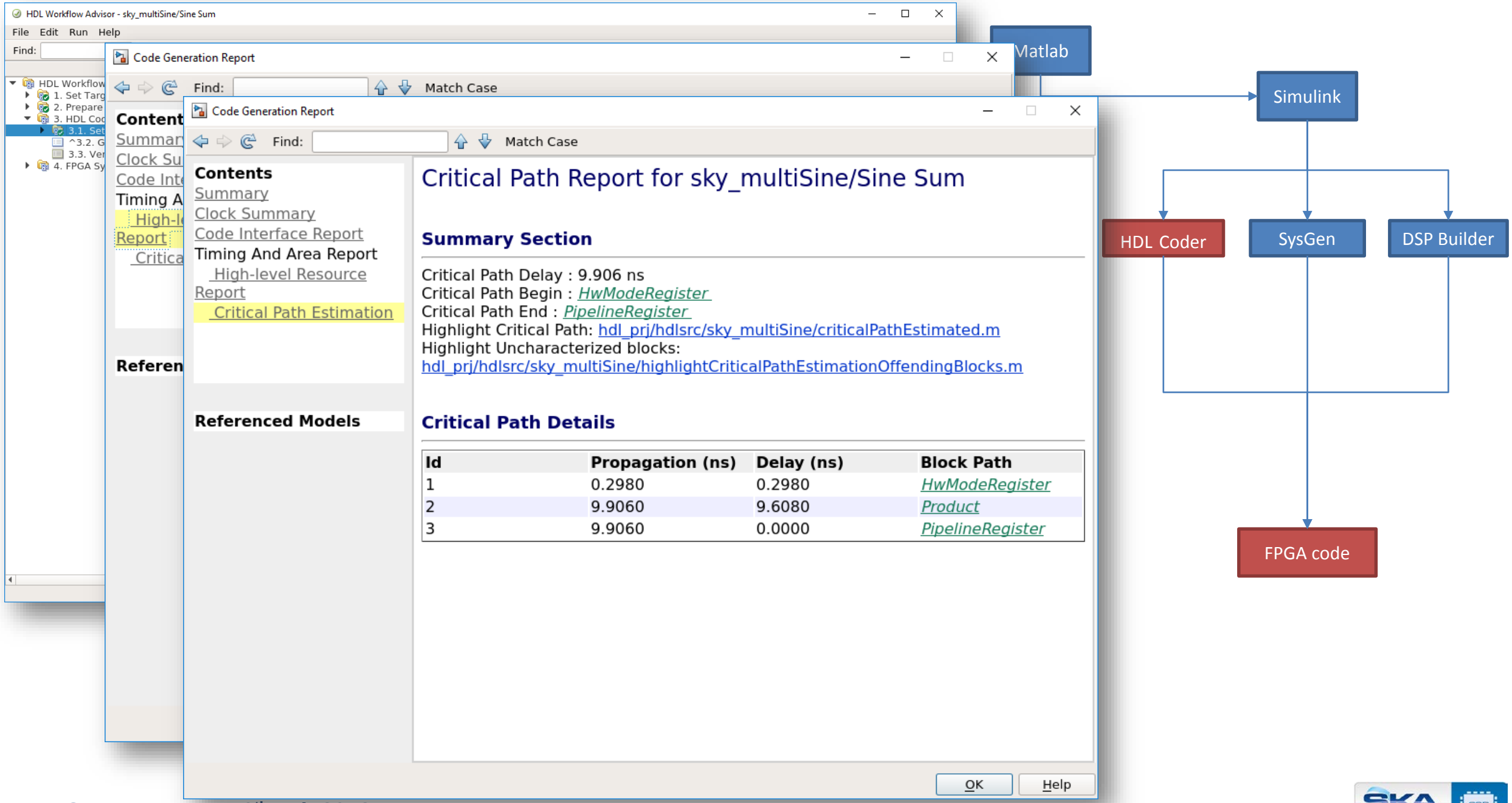
HDL Workflow Advisor - sky_multiSine/Sine Sum
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HDL Workflow
1. Set Targ
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3. HDL Cod
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3.3. Ver
4. FPGA Sy
Code Generation Report
Find:
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Code Generation Report
Find:
Match Case
Contents
Summary
Clock Summary
Code Interface Report
Timing And Area Report
High-level Resource Report
Critical Path Estimation
Referenced Models
Critical Path Report for sky_multiSine/Sine Sum
Summary Section
Critical Path Delay : 9.906 ns
Critical Path Begin : HwModeRegister
Critical Path End : PipelineRegister
Highlight Critical Path: hdl_prj/hdlsrc/sky_multiSine/criticalPathEstimated.m
Highlight Uncharacterized blocks:
hdl_prj/hdlsrc/sky_multiSine/highlightCriticalPathEstimationOffendingBlocks.m
Critical Path Details
Id | Propagation (ns) | Delay (ns) | Block Path
1 | 0.2980 | 0.2980 | HwModeRegister
2 | 9.9060 | 9.6080 | Product
3 | 9.9060 | 0.0000 | PipelineRegister
OK
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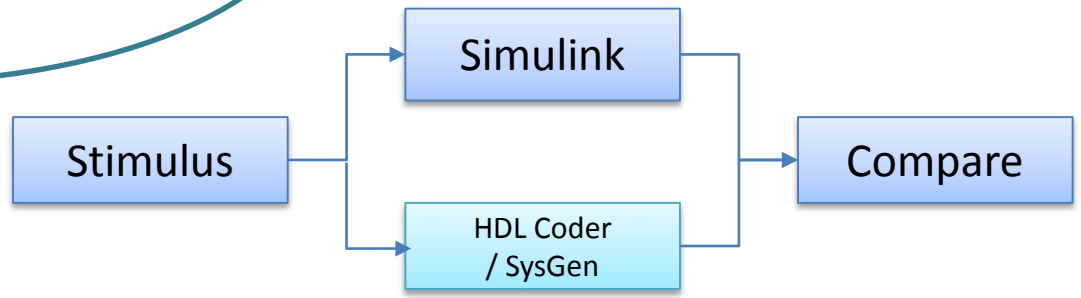

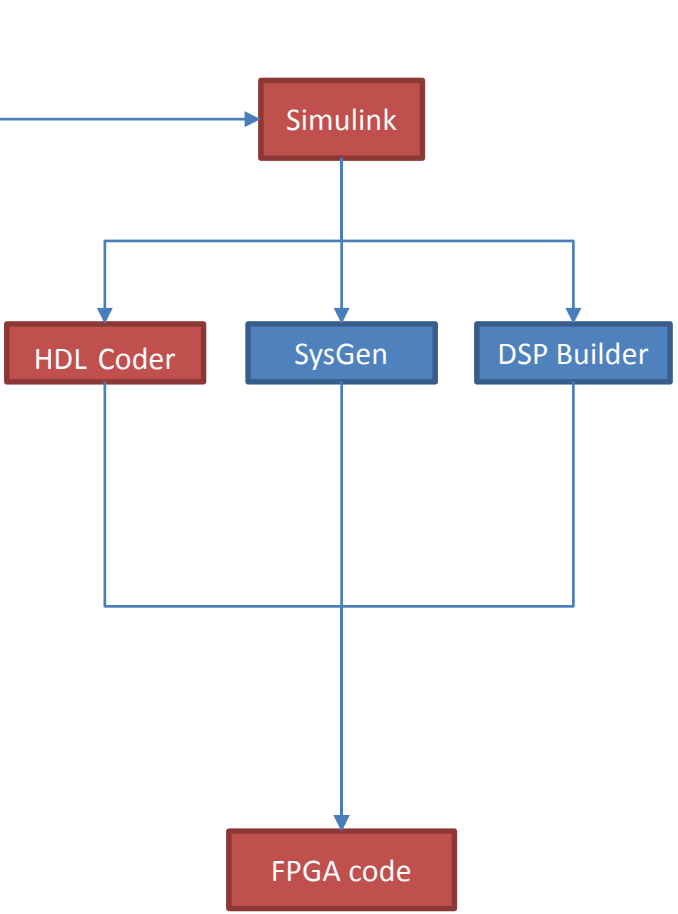

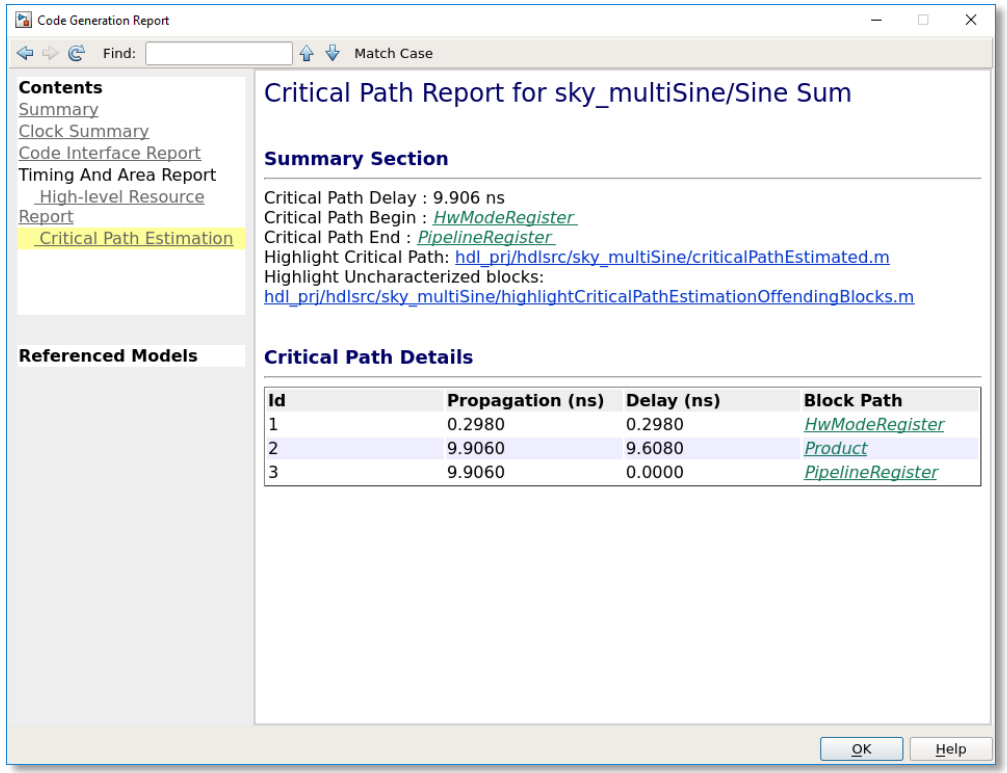
Code Generation Report

Find: Match Case

Contents

Summary
Clock Summary
Code Interface Report
Timing And Area Report
High-level Resource Report
Critical Path Estimation

Referenced Models

Critical Path Report for sky_multiSine/Sine Sum

Summary Section

Critical Path Delay : 9.906 ns
Critical Path Begin : *HwModeRegister*
Critical Path End : *PipelineRegister*
Highlight Critical Path: hdl_prj/hdlsrc/sky_multiSine/criticalPathEstimated.m
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hdl_prj/hdlsrc/sky_multiSine/highlightCriticalPathEstimationOffendingBlocks.m

Critical Path Details

Id	Propagation (ns)	Delay (ns)	Block Path
1	0.2980	0.2980	*HwModeRegister*
2	9.9060	9.6080	*Product*
3	9.9060	0.0000	*PipelineRegister*

OK Help

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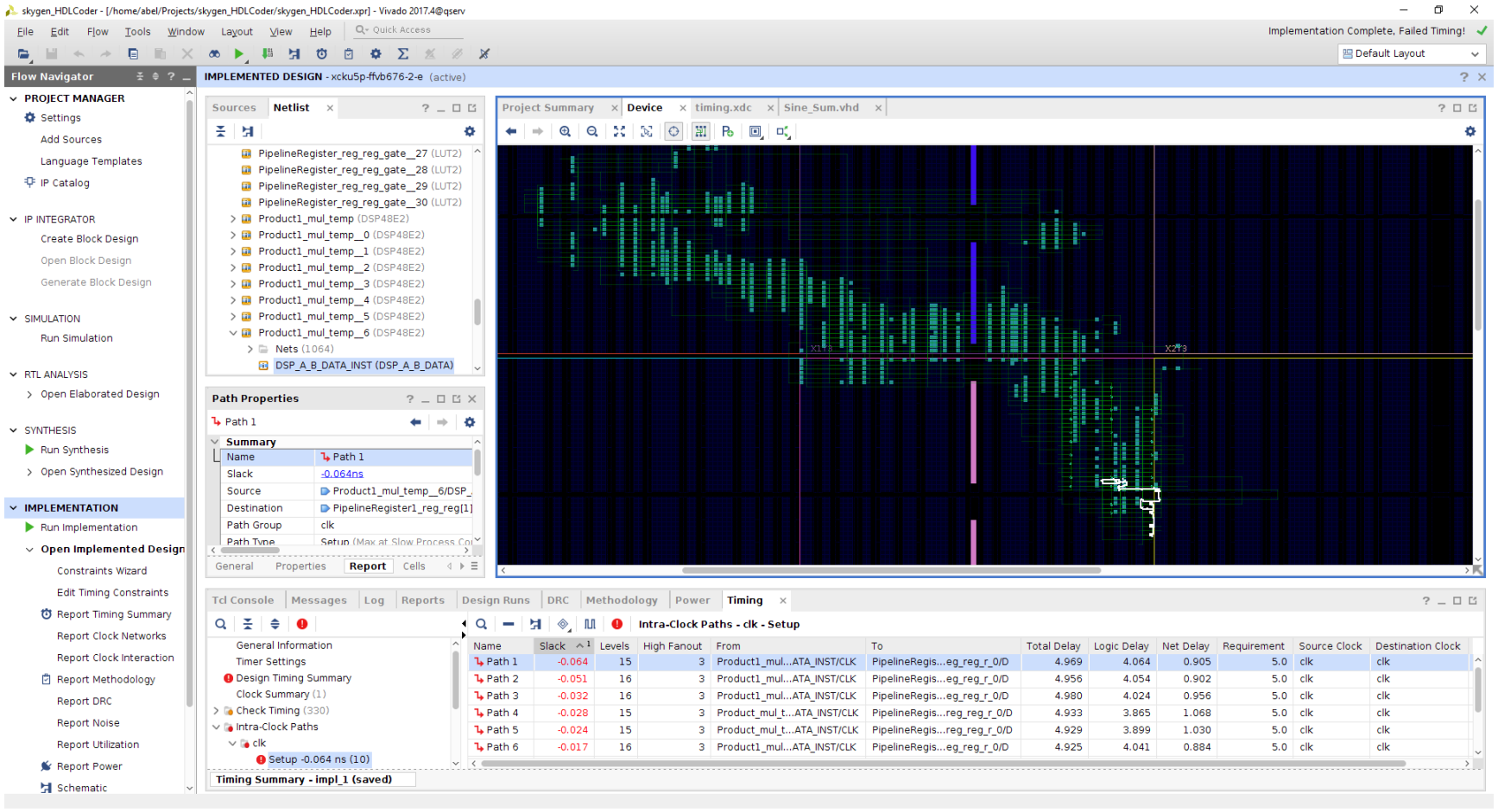
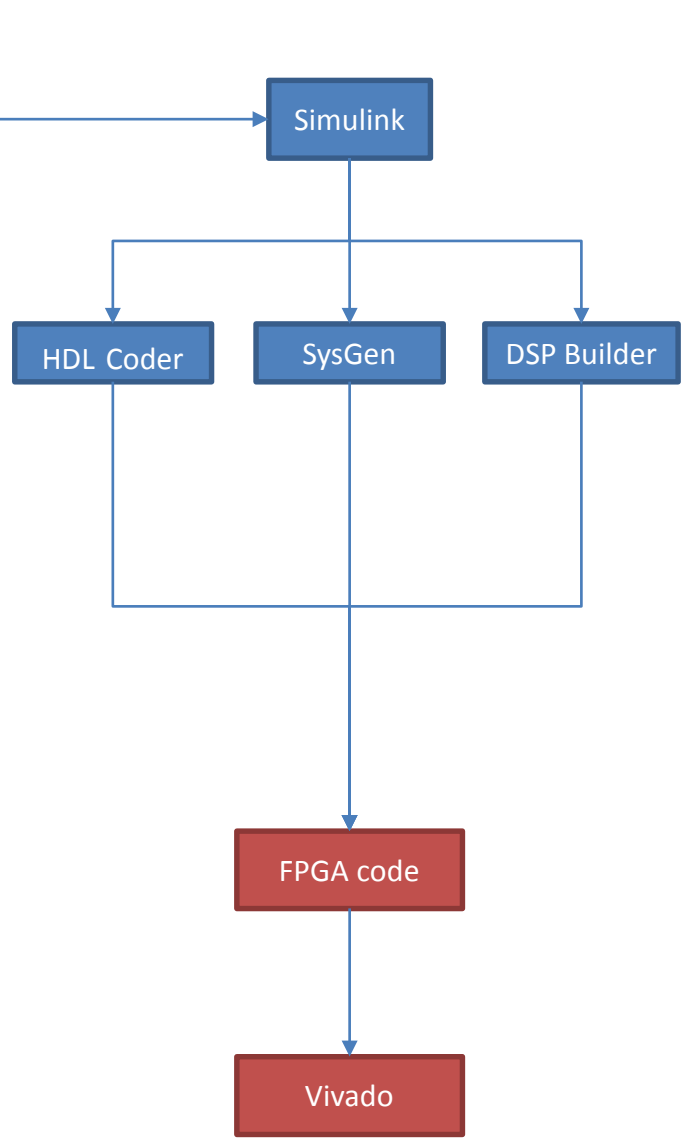
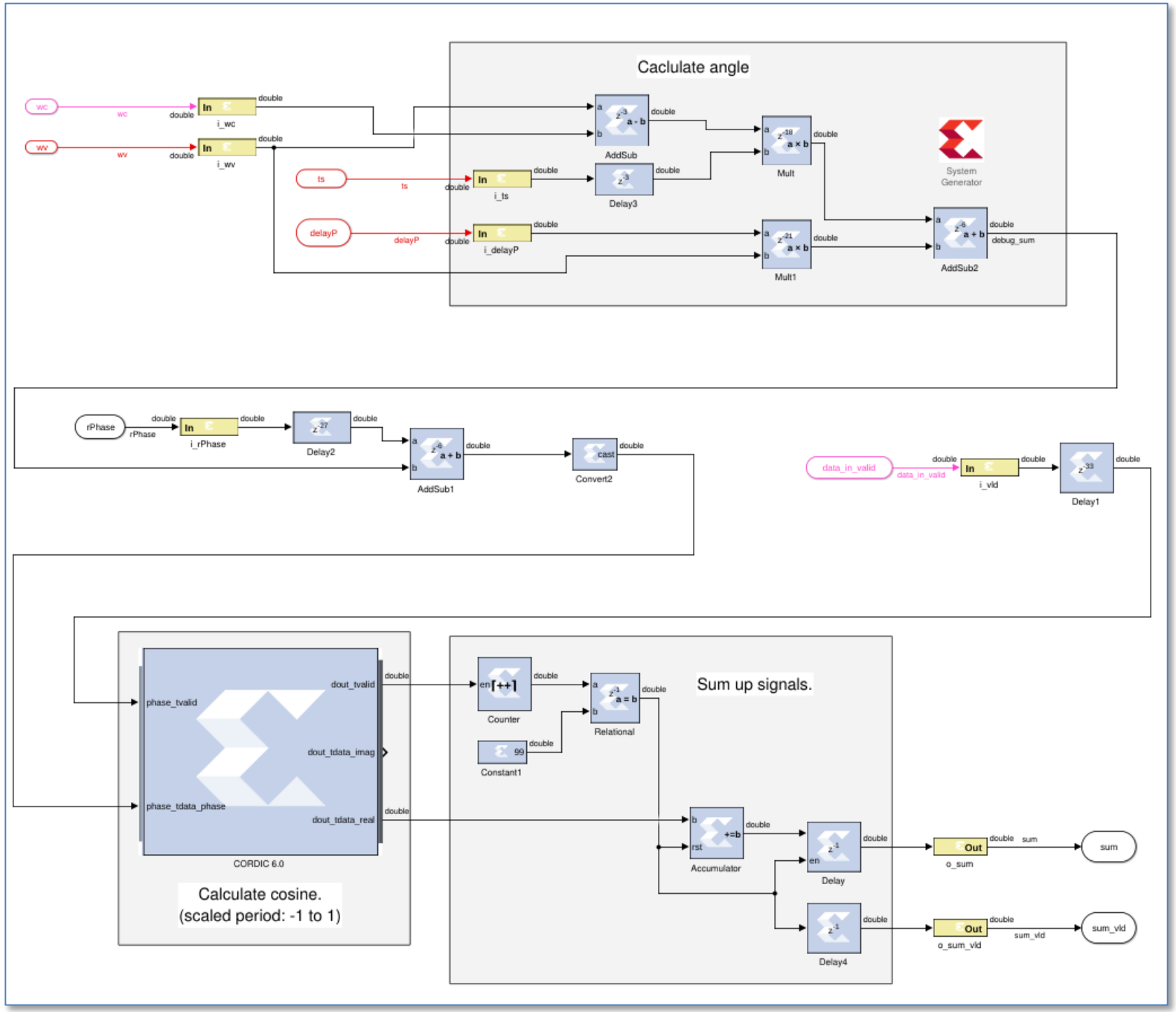
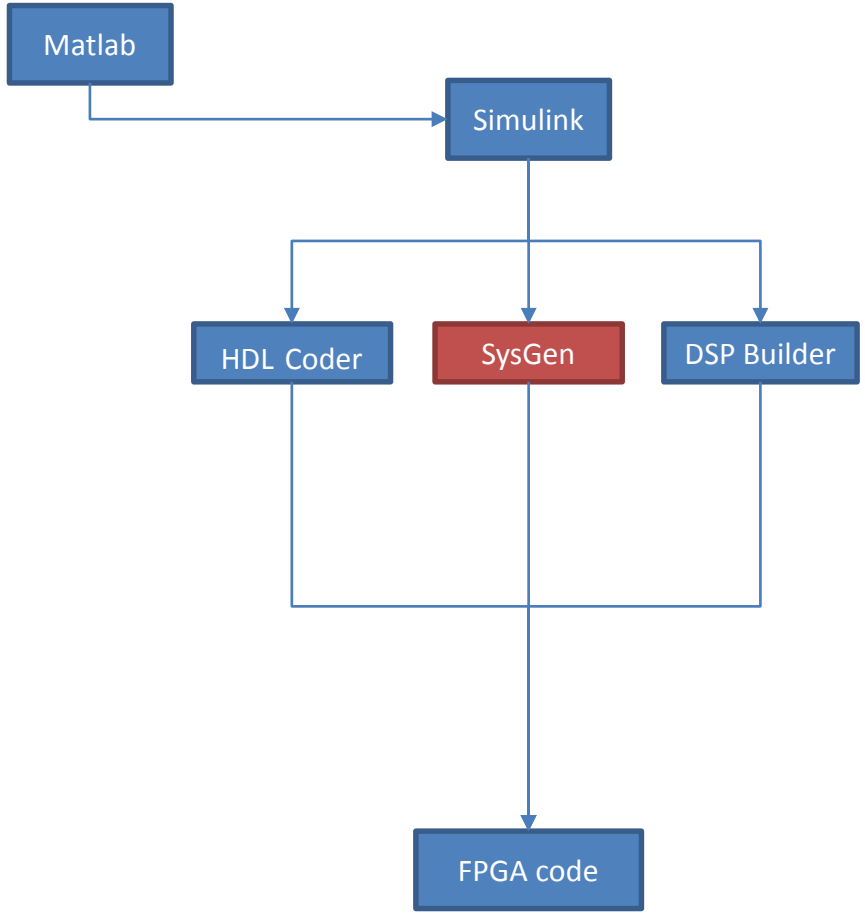





Caclulate angle
wc
wv
ts
delayP
i_wc
i_wv
i_ts
i_delayP
AddSub
Delay3
Mult
Mult1
AddSub2
System Generator
debug_sum
rPhase
i_rPhase
Delay2
AddSub1
Convert2
data_in_valid
i_vld
Delay1
phase_tvalid
phase_tdata_phase
dout_tvalid
dout_tdata_imag
dout_tdata_real
CORDIC 6.0
Calculate cosine.
(scaled period: -1 to 1)
Sum up signals.
Counter
Constant1
Relational
Accumulator
Delay
Delay4
o_sum
o_sum_vld
sum
sum_vld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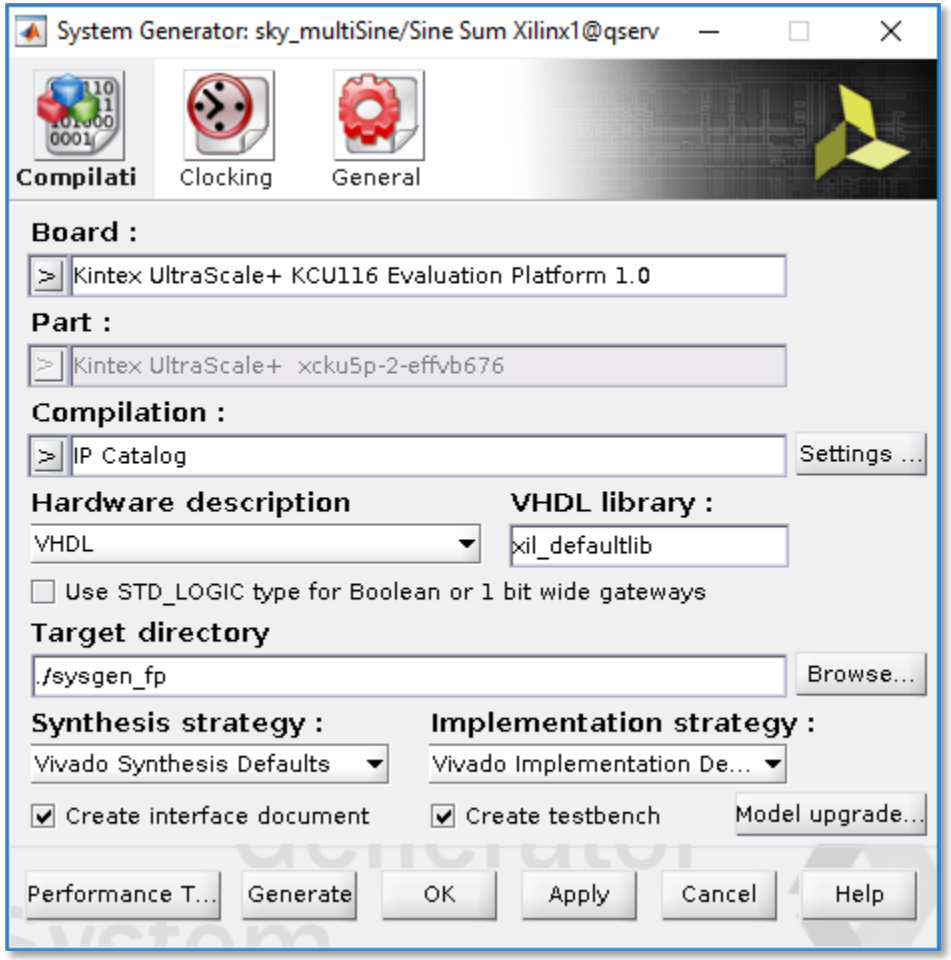

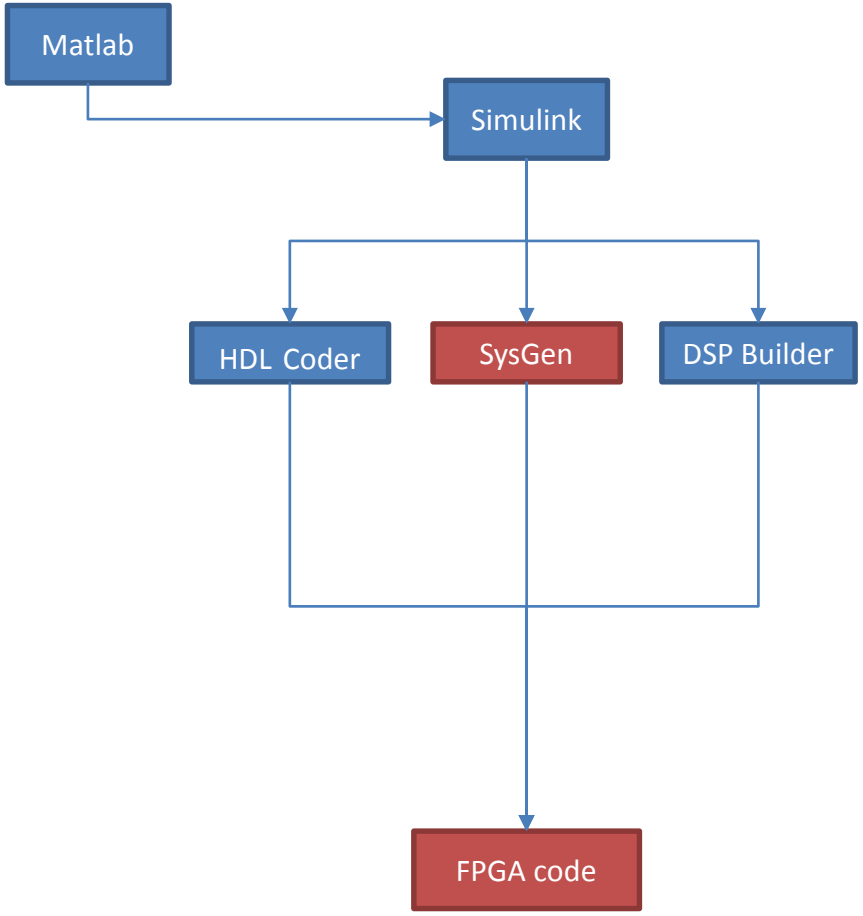

Summary / Comparison

	HDL Coder	SysGen
Starting Point	Simulink Subset	Simulink Subset
Frontend	Very Good	Very Good
Floating Point Support	NO	YES
Generated VHDL	Tidy	Almost Unreadable (but option “IP Catalog” allows to hide that)
Skygen Example DSP usage	32 (of 1824)	Float: 16 FP: 28
Skygen Example CLB LUTs usage	4292 (of 216,960)	Float: 6231 FP: 4514
Skygen Example Max Freq	~ 200 MHz	Float: ~ 280 MHz FP: ~ 280 MHz